Semifore

Total Register Automation

A Winning Methodology

Semifore's CSRSpec™ language and CSRCompiler™ system form is a scalable and robust methodology to automate hardware/software interface design, verification, firmware, and documentation.

CSRCompiler provides multi-language support without the need for additional scripting. In response to customer requests, CSRSpec continues to provide functionality not available in IP-XACT or SystemRDL. The methodology supports an agile design process to ensure best practices and early engagement by the entire design team.

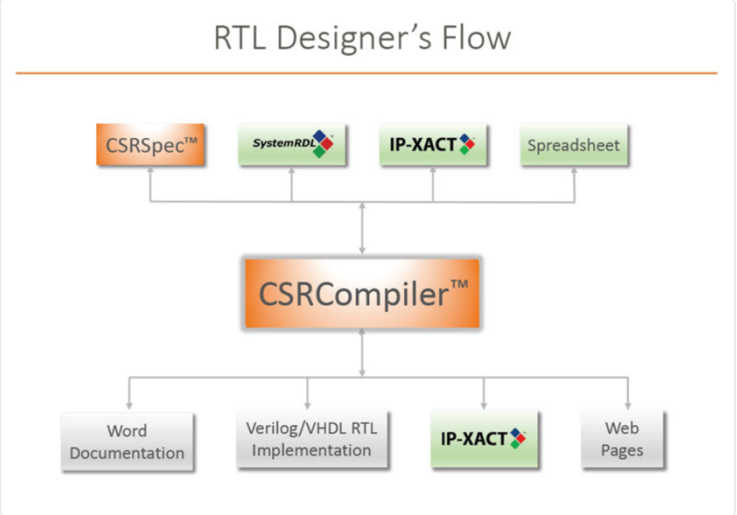
CSRCompiler identifies IP integrity issues to ensure clean import of third-party IP or internal legacy data. It performs a strict lexical analysis, parse tree evaluation, and semantic check of third-party files. The semantic checking extends beyond standards to ensure the address map is self- consistent and will allow the generation of valid RTL.

Solving Address Map Complexity

SoC designs have reached tens of thousands of configuration and status registers – in some cases two or three orders of magnitude more – on a single chip. With these thousands of registers have come substantial design challenges, with productivity and design integrity at the forefront. The Semifore methodology works at the register behavior level of abstraction, in the architectural design phase, to solve these problems. Design intent is specified with CSRSpec and is implemented in a flexible address map hierarchy. It provides an intuitive management system that processes the register specification, or address map of the design. These address maps are the behavioral foundation for the chip that ultimately define its functionality, performance and behavior.

Documentation

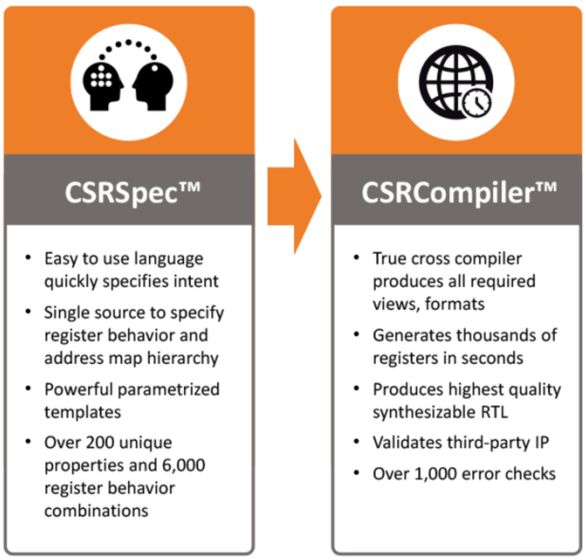
The Semifore methodology documents changes across entire functional teams, ensuring a reliable, up-to-date specification is being used at all times. It provides a single-source specification for register and memory-map information fully configured for all teams in the formats and views they require. All teams – functionally diverse and geographically separate – remain synchronized.



Single Source Methodology

The Semifore methodology is unique in that many aspects of the design originate from a single source. CSRCompiler generates synthesizable RTL at the push of a button. It also generates documentation across design teams

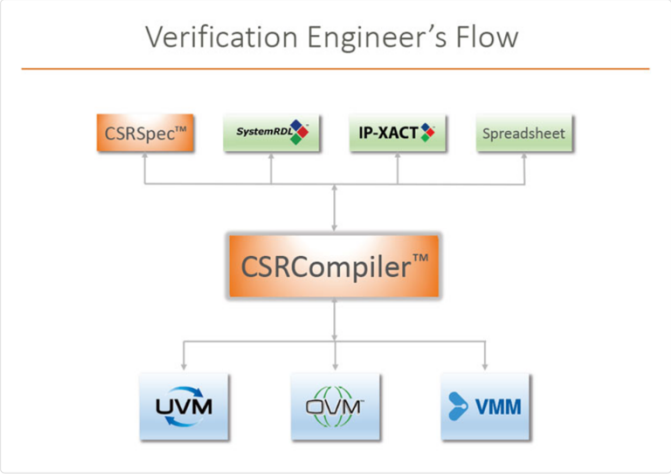
Semifore Methodology



while ensuring all Information is correct. It is extremely flexible and allows multiple input formats to be linked to create the single source, and it provides customized output for the individual needs of the entire design team.

CSRCompiler

The power behind the Semifore methodology, CSRCompiler provides orders-of-magnitude performance improvements while solving complex SoC issues. It is a true cross compiler with over 1,000 functional, behavioral, syntactic, and semantic error checks. It is extremely fast and generates superior quality synthesizable RTL. Proven to compile over one million configuration and status registers in minutes, CSRCompiler automates the views and formats for register design. Innate to the compiler is its ability to validate intellectual property from third-party or internal legacy data, ensuring data is clean and ready for use.



CSRCompiler accepts IP-XACT, SystemRDL, spreadsheets and CSRSpec to generate both industry standard output and output customized for design teams.

- True cross compiler produces all required views, formats
- Generates thousands of registers in seconds
- Produces highest quality synthesizable RTL
- Validates third-party IP
- Over 1,000 error checks

CSRSpec Language™

Created by Semifore, the CSRSpec language provides a single source to specify register behavior and address map hierarchy of a chip. A defacto standard among many customers, it is a terse and easy to understand language. It includes over 200 unique properties and 6,000 register behavior combinations. When compiled, the language expands to a full implementation high quality RTL ready for synthesis. CSRSpec also provides configurable parameterized templates to promote design reuse and consistency between teams.

- Easy to understand language implements superior synthesizable RTL
- A single data source to generates RTL, firmware headers, verification class instances, and documentation outputs
- Promotes repeatability, scalability and legacy data reuse
- Natively interfaces with industry standards and those not currently available (bus, memory, wide data paths)

Contact us for an evaluation

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