A 3.2 Gbps/pin HBM2E PHY with Low Power I/O and Enhanced Training Scheme for 2.5D System-in-Package Solutions

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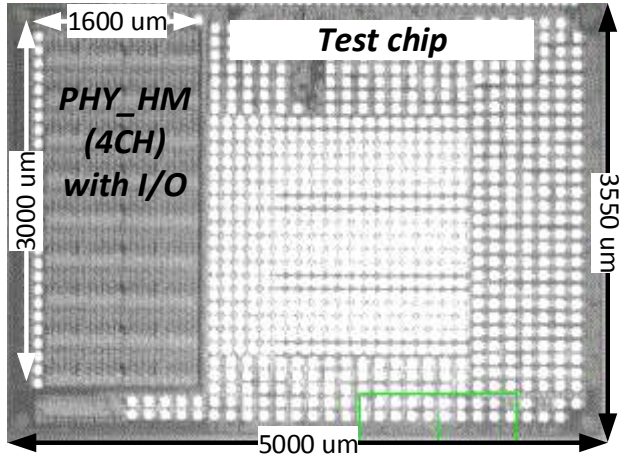
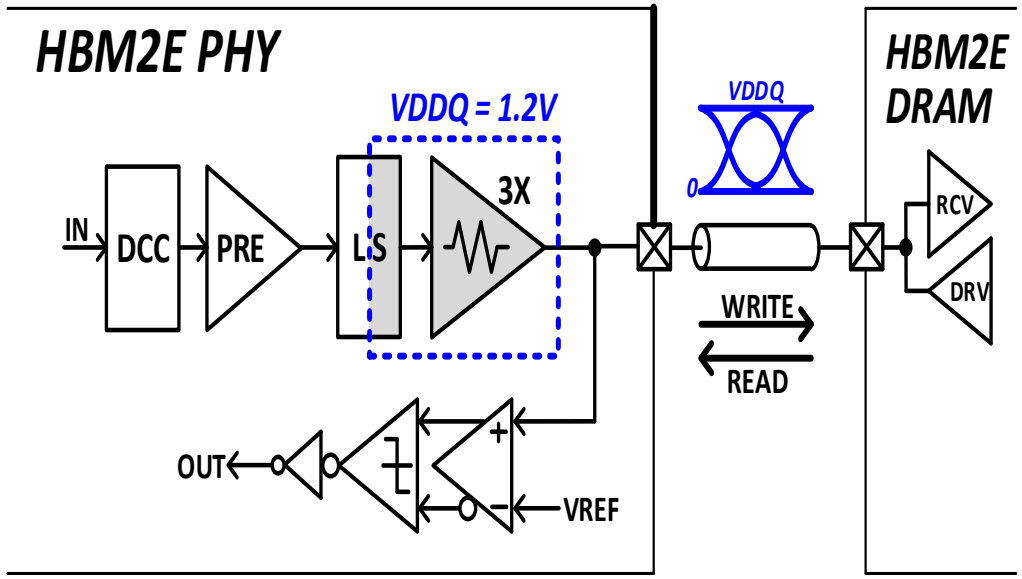
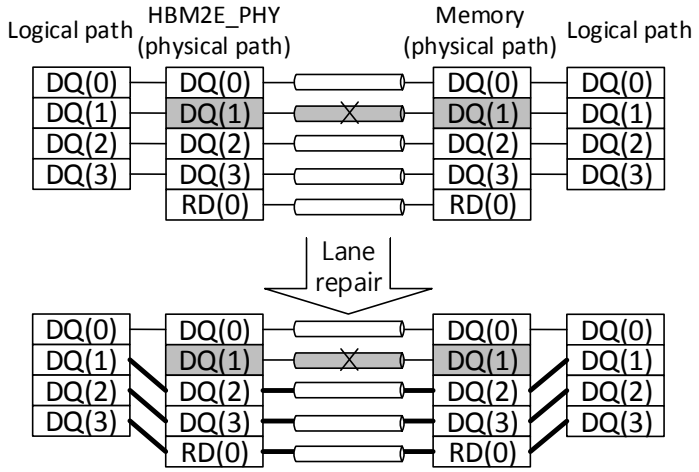
Abstract

- *3.2 Gbps/pin HBM2E PHY IP implementation*
  - *Low power I/O scheme (1.07 pJ/bit@write operation)*
    - *Minimize the number of blocks using VDDQ power*
  - *Training scheme using redundancy bits (~7% VWM gain)*
    - *Redundancy pins are used as candidates@initial training*







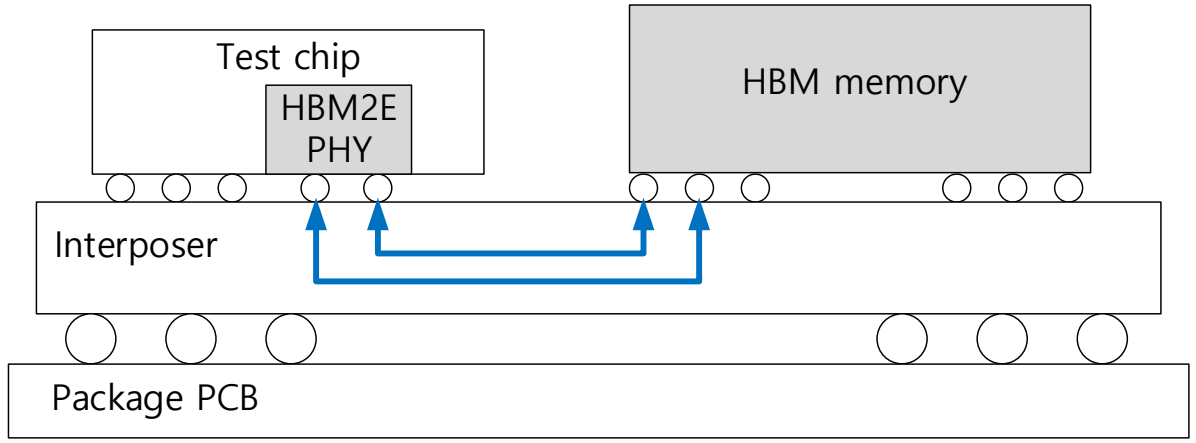
$$\hat{x}_{excluded\_DQ}(i) = \underset{x_i \in [0,15]}{\arg\min} VWM(DQ(x_i)), i = 0, \dots, 63$$

Outline

- **Introduction**
  - HBM introduction and test chip for HBM2E PHY
- **Low power I/O**
  - Structure of driver and receiver
- **Training scheme considering redundancy pins**
  - Training flow chart
- **Measurement Results**
  - Implementation and power measurement results
  - Valid window margin results

Introduction

- **HBM2E (High Bandwidth Memory) [1,2]**
  - → 1024 pins@>2.8Gbps (>358.4GB/s), 128bit/channel, 32bit/DQS
  - → 8CH/device (VDDQ (1.2V), VDDC(1.2V))
  - → # of stack/chip: 4H/8H
  - → Application: HPC, Server



[1] JEDEC Standard High Bandwidth Memory (HBM) DRAM Specification, Standard JESD235B, 2015.
[2] Dong Uk Lee et al., "A 1.2 V 8 Gb 8-Channel 128 GB/s High-Bandwidth Memory (HBM) Stacked DRAM With Effective I/O Test Circuits", *IEEE Journal of Solid-State Circuits*, Vol.50, Issue 1, 2015, pp. 191-203.

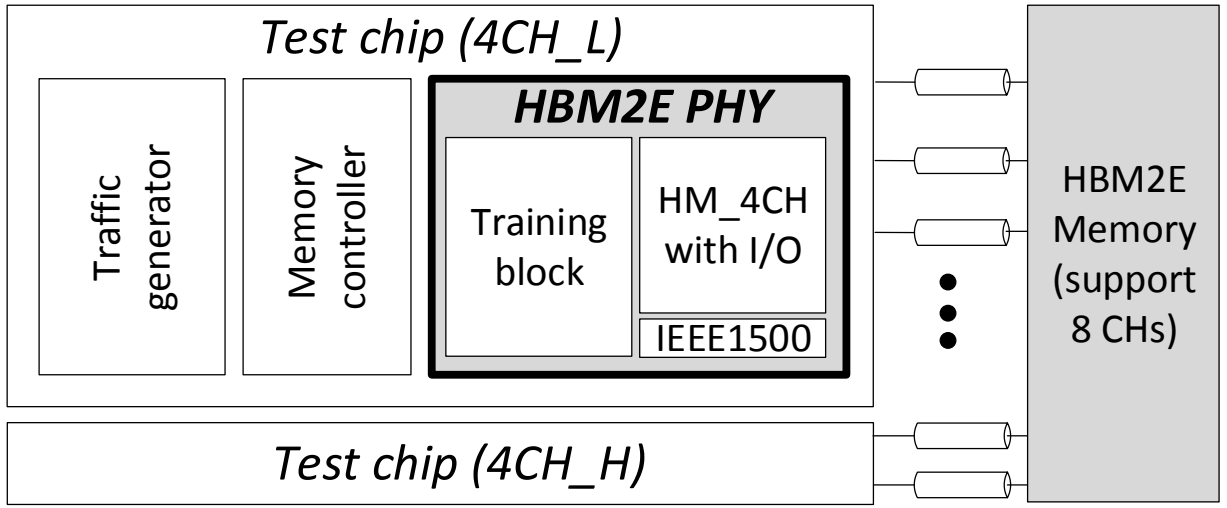
Test chip for HBM2E PHY

- **Test chip structure**

  → Two test chips and one HBM memory chip are integrated on single silicon interposer

  → Test chip includes one **HBM2 PHY** for 4CH and test logics such as traffic generator and memory controllers

  → Traffic generator has several DMAs and one RTIC*



* RTIC (Run Time Integrity Checker)

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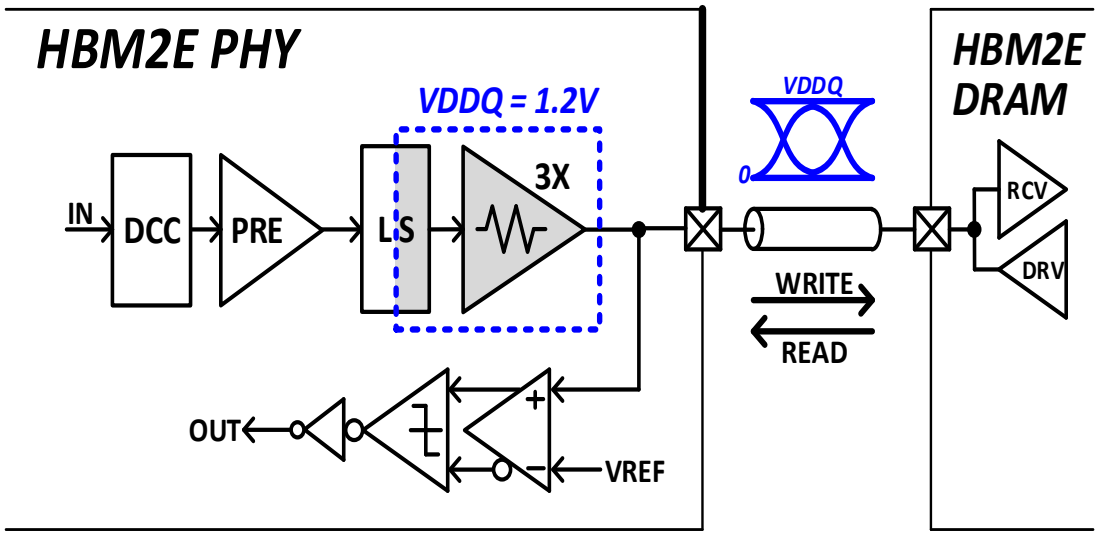
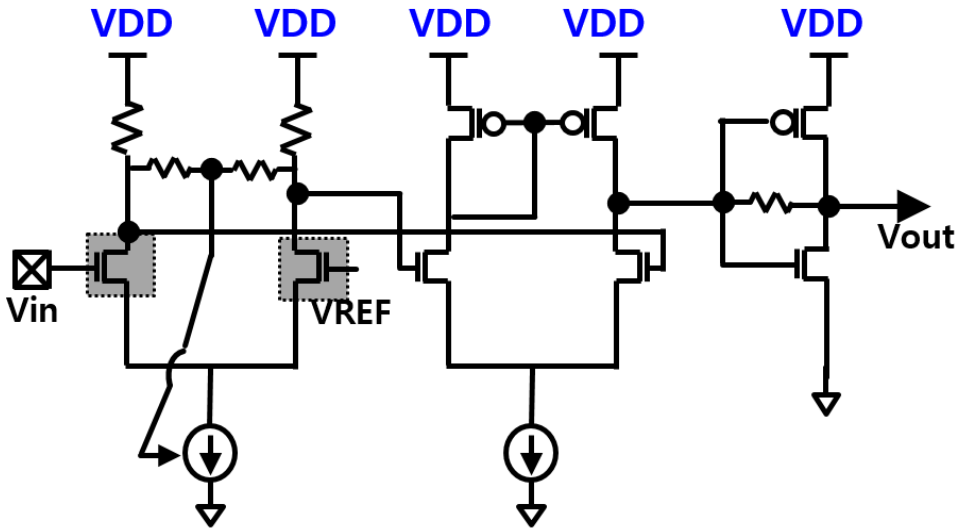
Low power I/O

- Minimize the number of blocks using VDDQ power by moving level shifter (LS) from input side of pre-driver to output side [3]
- Receiver uses only VDD power and it is designed to minimize the number of stages (2stage)



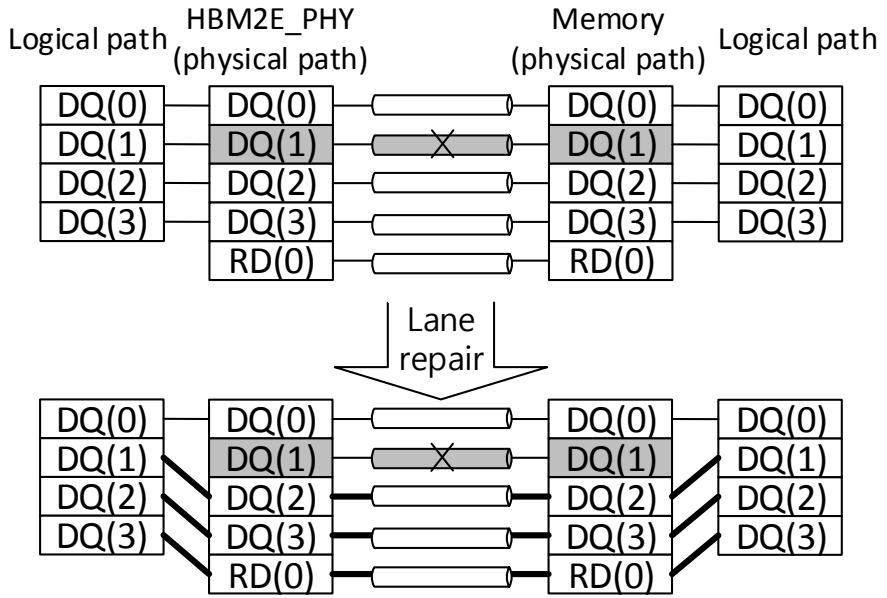
<Top and Driver>

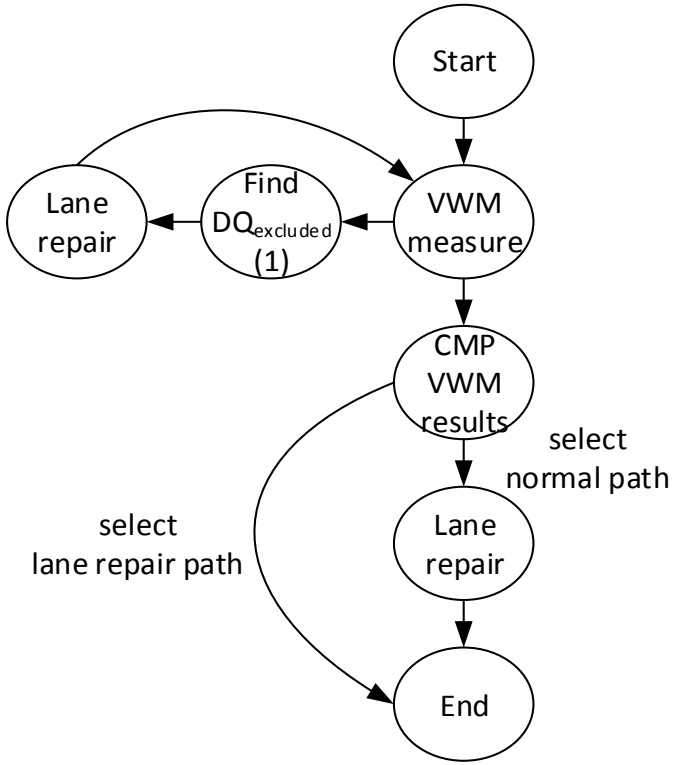


<Receiver>

[3] Soo-Min Lee et al., "A 0.6V 4.266Gb/s/pin LPDDR4X Interface with Auto-DQS Cleaning and Write-VWM Training for Memory", *ISSCC*, 2017, pp. 397-399.

Training scheme including redundancy pins





$$\hat{x}_{excluded\_DQ}(i) = \underset{x_i \in [0,15]}{\arg\min} VWM(DQ(x_i)), i = 0, \ldots, 63$$

- Motivation is to reduce performance variation among DQ pins which can be caused by PI (Power Integrity) and SI (Signal Integrity)
- Main idea is to include redundancy pins when performing training even though there are no defects

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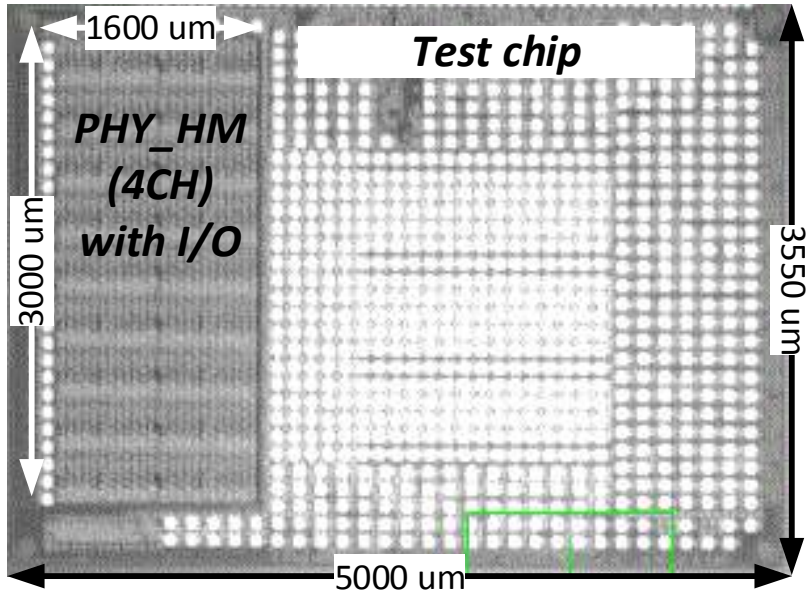
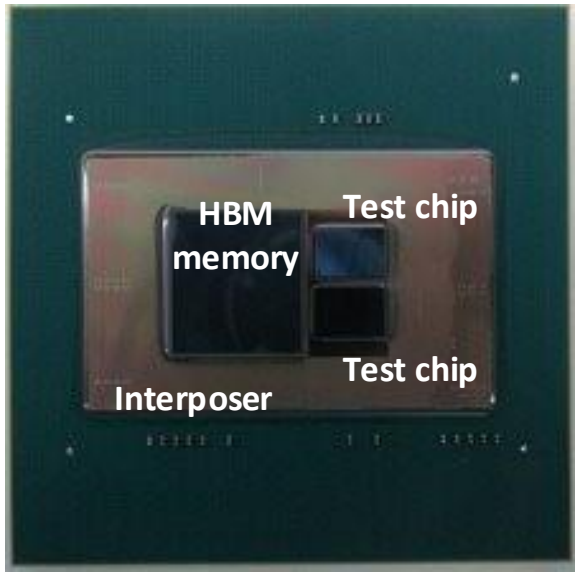
Implementation results

- Test chip size is 5 x 3.55 mm^2 and implemented with 7nm fabrication process
- Two chips and one HBM memory are integrated on single interposer
- Except for training block, HBM PHY with IO for 4CH is 1.6 x 3 mm^2



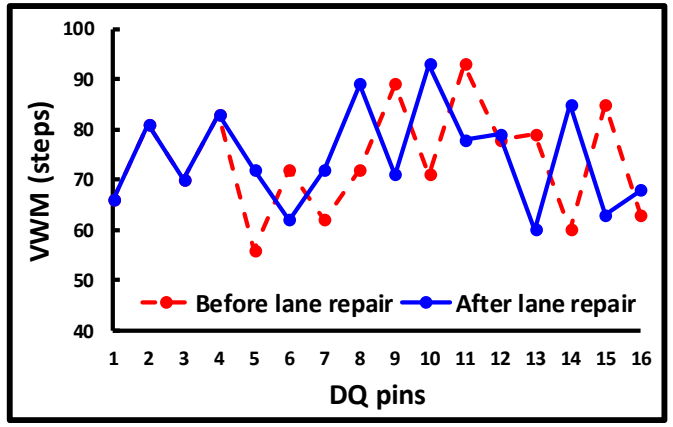


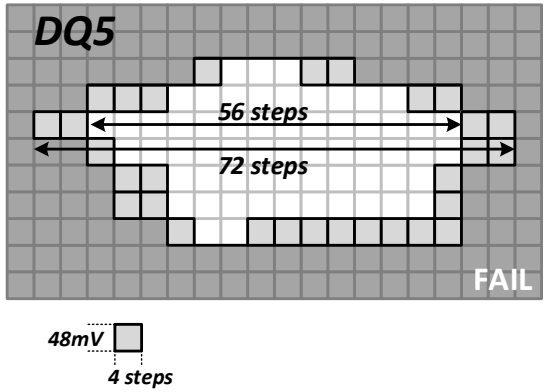
Power and VWM measurement results

- 1.07 pJ/bit @ write operation (HM and I/O)

0.75V/1.2V/8CH	WRITE	READ	IDLE
HM	810	1480	36
I/O	2700	1130	14
Energy [pJ/b]	1.07	0.56	0.02

- Approximately 7% VWM enhancement





Conclusion

- **3.2Gbps/pin HBM2E PHY is implemented in 7nm**
  → PHY is verified on 2.5 SiP test chip
- **Low power I/O**
  → Minimize the number of blocks using VDDQ
- **Performance**
  → Training scheme including redundancy pins
- **1.07pJ/bit@WRITE and 7% VWM enhancement**