Fully Autonomous Mixed Signal SoC Design & Layout Generation Platform

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Tutu Ajayi[*], Yaswanth K Cherivirala[*], Kyumin Kwon[*], Sumanth Kamineni[†], Mehdi Saligane[*], Morteza Fayazi[*], Shourya Gupta[†], Chien-Hen Chen[†], Dennis Sylvester[*], David Blaauw[*], Ronald Dreslinski Jr[*], Benton Calhoun[†], David D. Wentzloff[*]

* University of Michigan, Ann Arbor, MI
† University of Virginia, Charlottesville, VA

Abstract

We present FASoC, the world's first autonomous mixed-signal SoC framework driven entirely by user constraints, along with a suite of automated generators for analog blocks. The process-agnostic framework takes high-level user intent as inputs to generate optimized and fully verified analog blocks using a cell-based design methodology.

Our approach is highly scalable and silicon-proven by an SoC prototype which includes 2 PLLs, 3 LDOs, 1 SRAM, and 2 temperature sensors fully integrated with a processor in a 65nm CMOS process. The physical design of all blocks, including analog, is achieved using optimized synthesis and APR flows in commercially available tools. The framework is portable across different processes and requires no-human-in-the-loop, dramatically accelerating design time.

Background

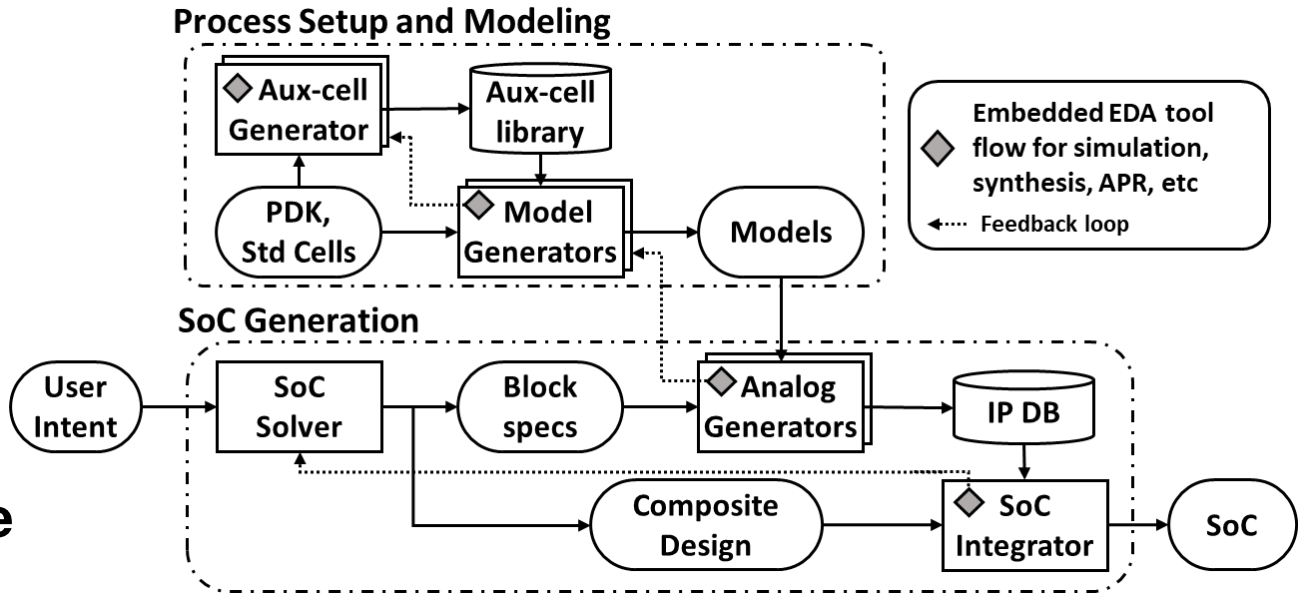
- **Motivation**
  - A typical SoC has many analog components, which have labor intense design processes
  - Modern SoCs have more functional blocks (in number and variety)
  - Custom Layout is more challenging in advanced nodes (<28nm)
  - Quickly and correctly integrating several blocks into a single SoC is challenging

- **Goals**
  - A single SoC design tool that produces RTL descriptions for both analog and digital components
  - Cell-based design methodology for synthesizing custom analog blocks
  - Correct-by-construction SoC build-up using IP-XACT descriptions of RTL
  - A PDK and EDA tool vendor agnostic approach
  - Provide a suite of analog generators (PLL, LDO, Temperature sensor, SRAM)
  - A harness to support more generator types and 3rd Party IP
  - Hands-free synthesis+APR for the entire SoC design with fabricable GDS2 layout

- **Impact**
  - An autonomous *silicon compiler* that reduces the complexity of realizing modern SoCs on advanced nodes and cuts down on design time.

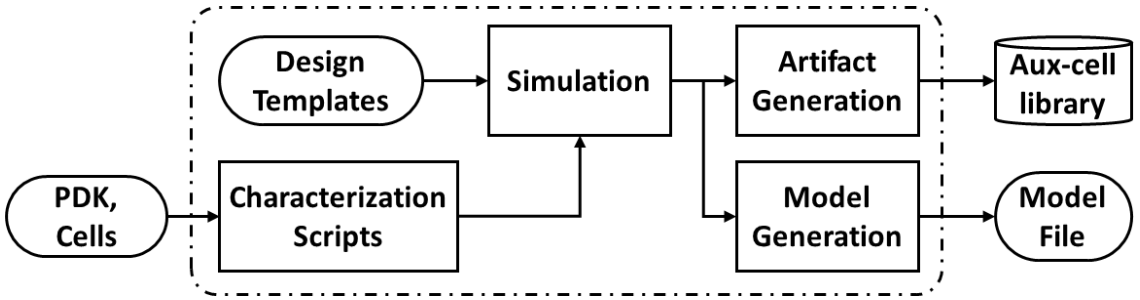
Introduction: FASoC Framework Overview

- **Process setup and modeling**
  - Generation of the aux-cells and models for the analog generators
  - Performed once for the process design kit (PDK)
- **SoC generation phase**
  - Translates high-level user-intent into analog specifications that satisfy the user constraints.
  - The analog block generators are invoked as needed to create bespoke IP blocks
  - SoC integrator stitches together the composite design
  - Performs synthesis and APR flow to create the final SoC layout

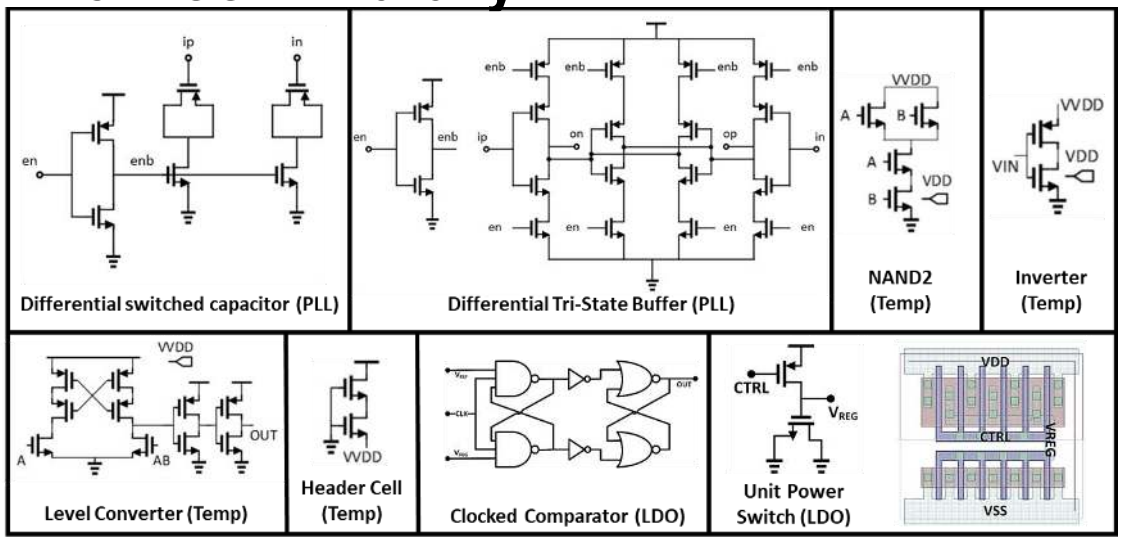


FASoC: Process Setup and Modeling

- **Aux-cell generation**
  - These are small analog cells with specific analog functionality used in conjunction with std cells
  - Derived from a template and characterized/optimized per process
  - Currently laid out manually



- **Aux-cell Library**



- **Modeling**
  - The modeling for each generator is automated and vary in implementation using a combination of mathematical equations, machine learning, and design space exploration

FASoC: SoC Generator

1. **SoC solver**
   - Determines the optimal *composite design* which is a combination of blocks, analog specifications, and connections as translated from user intent

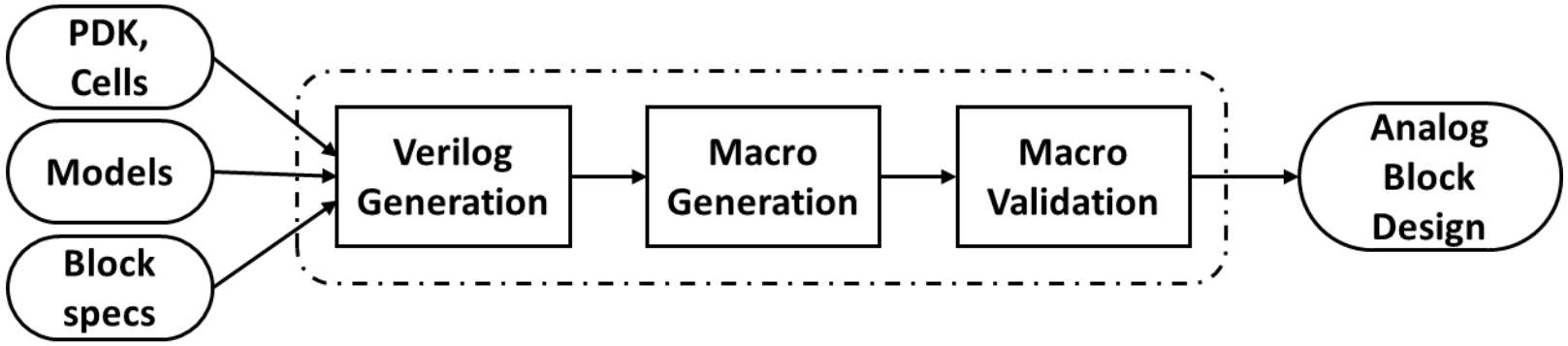
2. **Analog Block Generation**
   - Invokes generators to create bespoke blocks
   - Results are in standard EDA file formats (lib, lef, gds, cdl, etc)
   - Results are also described in IP-XACT format

3. **IP Database**
   - Generators results are cached in a database for improved runtime
   - Includes 3rd party IPs such as processors and other peripherals

4. **Design stitching and composition**

5. **Adaptable synthesis and APR flow to generate final layout and perform validation (DRC/LVS)**

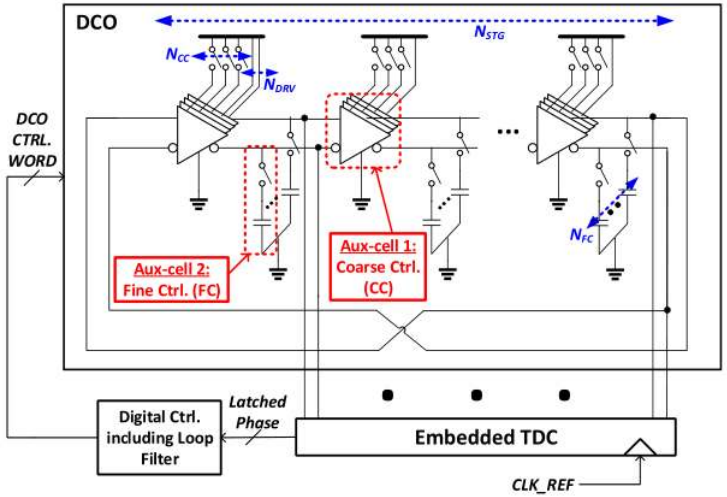
SoC Generator: Generic Analog Generator Flow



- **Verilog Generation**
  - Generate synthesizable Verilog description of the block that conforms to the input specs
  - Generate guidance information in a vendor-agnostic format
  - Generate pre-layout performance estimates
- **Macro Generation**
  - Convert guidance into vendor specific format/commands
  - Perform synthesis, APR, DRC, and LVS
  - Planned support for open-source EDA tools
- **Macro Validation**
  - Perform parasitic extraction, simulation and validation
  - Generate detailed datasheet report

Analog Generators: PLL

- **Block Architecture**
  - A ring oscillator based ADPLL

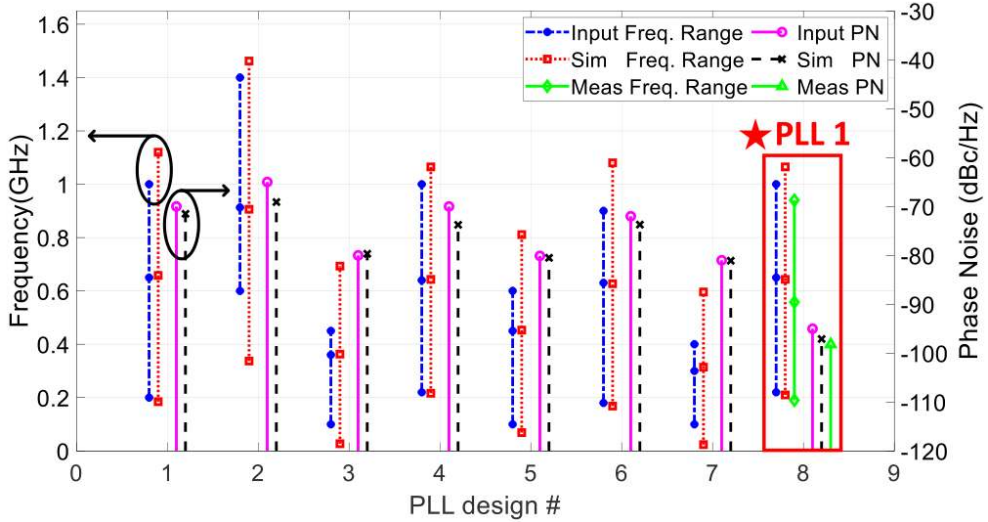


- **Aux Cells:**
  - Differential Switched Capacitor
  - Differential Tristate Buffer

- **Input Specifications**
  - Nominal Frequency Range
  - In-band Phase Noise

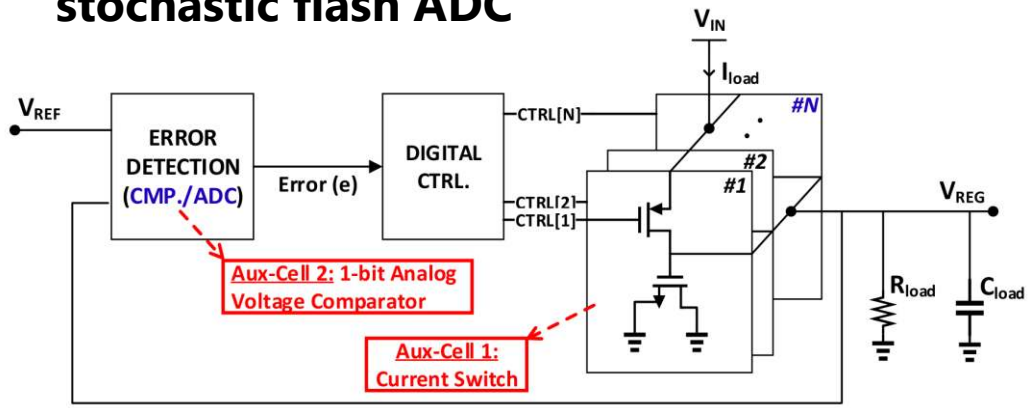
- **Generator Model**
  - Physics-based mathematical model

- **Generator Results**
  - Generated PLL designs for eight different input specifications.



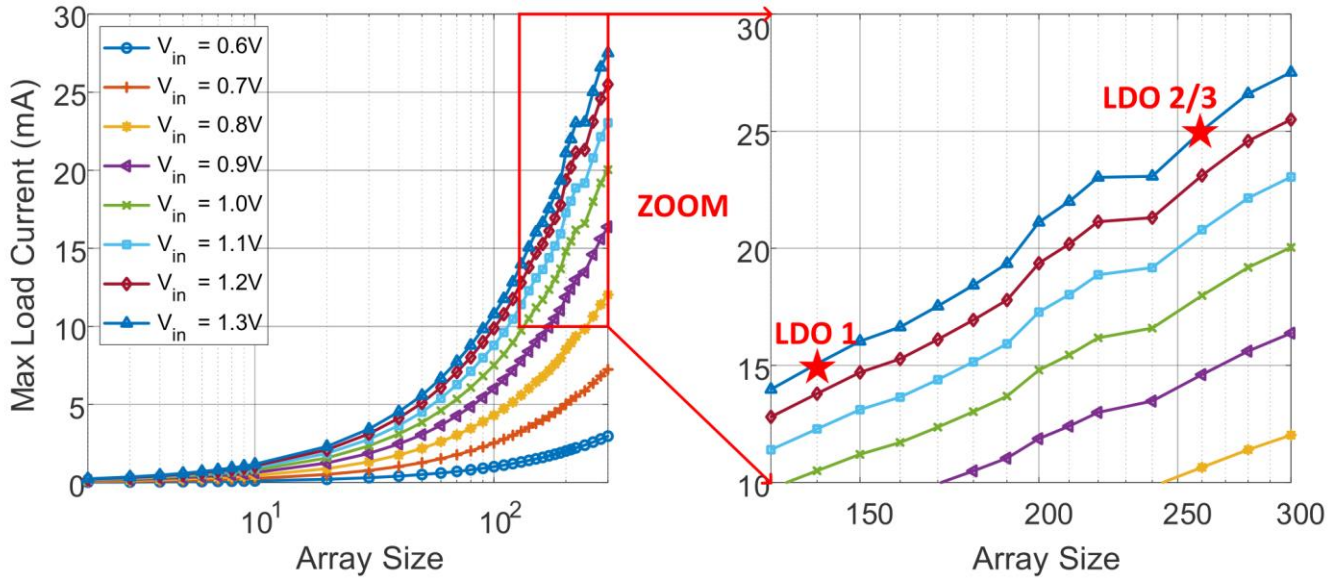
Analog Generators: LDO

- **Block Architecture**
- **Synchronous Digital LDO with optional stochastic flash ADC**



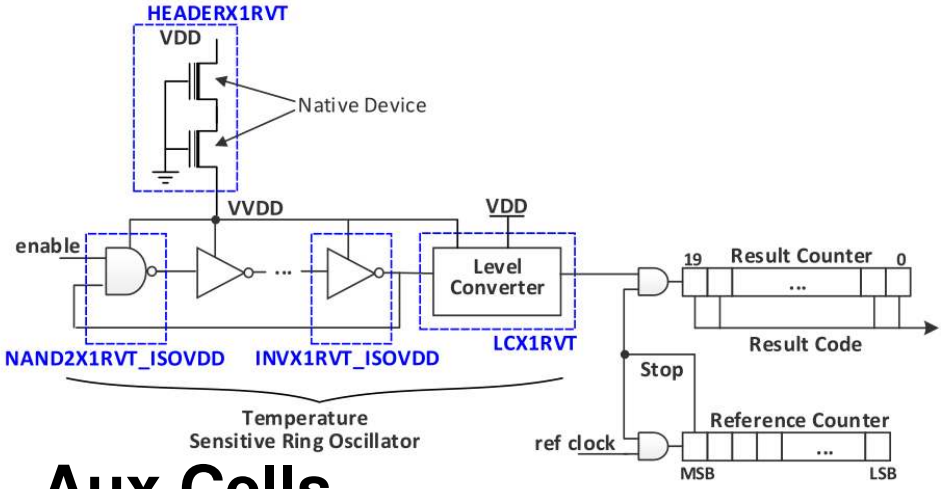
- **Aux-cells**
  - Clocked comparator
  - Unit power switch
- **Input Specifications**
  - V_{IN} Range
  - $I_{load,max}$ range
  - Dropout Voltage

- **Generator Model**
  - Poly-fit model
- **Generator Results**
  - $I_{load,max}$ vs. array size, for multiple LDO designs generated



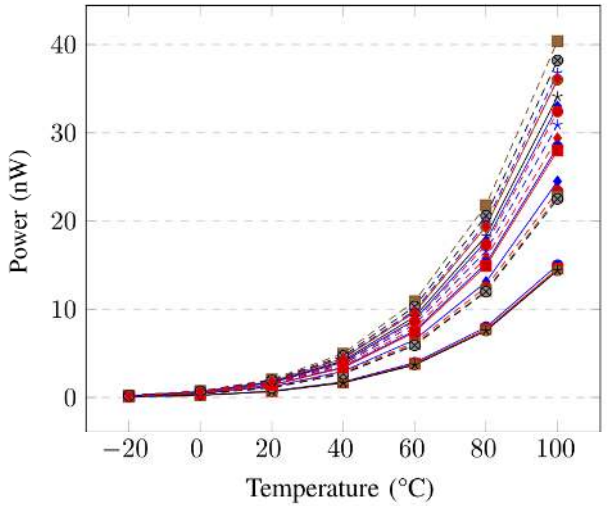
Analog Generators: Temperature Sensor

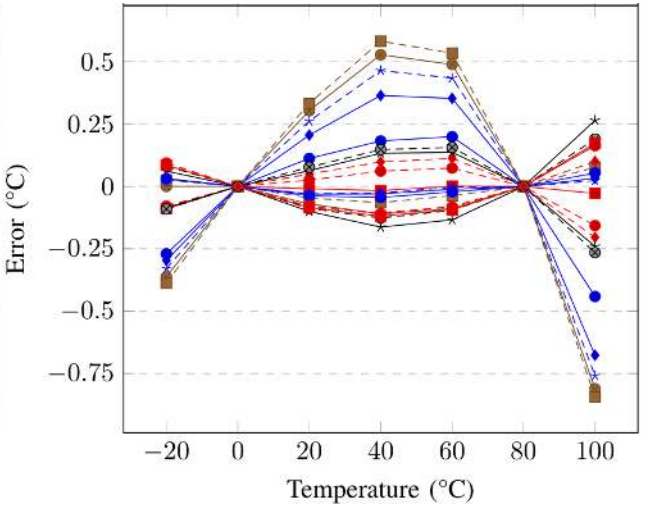
- **Block Architecture**
  - Temperature-sensitive ring oscillator and stacked zero-VT devices



- **Aux Cells**
  - Inverter
  - Level converter
  - Header cells
- **Input Specifications**
  - Temperature range
  - Optimization strategy

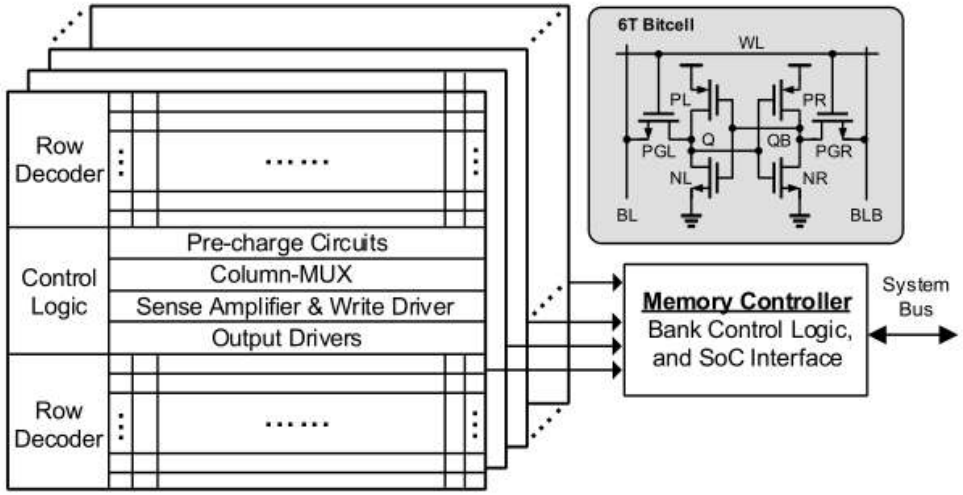
- **Generator Model**
  - Predictive Bayesian neural network model
- **Generator Results**
  - Power and Error results against temperature for various temperature sensor designs (each fitted plot represents a unique design)





Analog Generators: SRAM

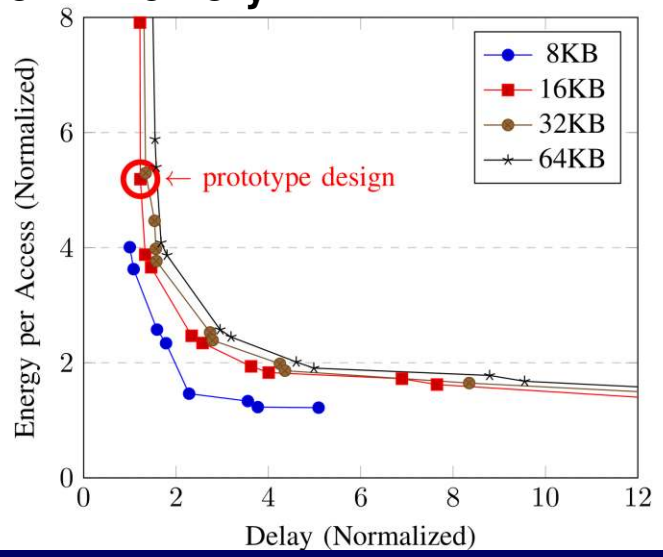
- **Block Architecture**
  - Standard multi- bank memory



- **Leverages Aux Macros**
  - 6T Bitcell, Row decoder, column mux, wordline driver, sense amplifier, write driver and pre-charge circuit

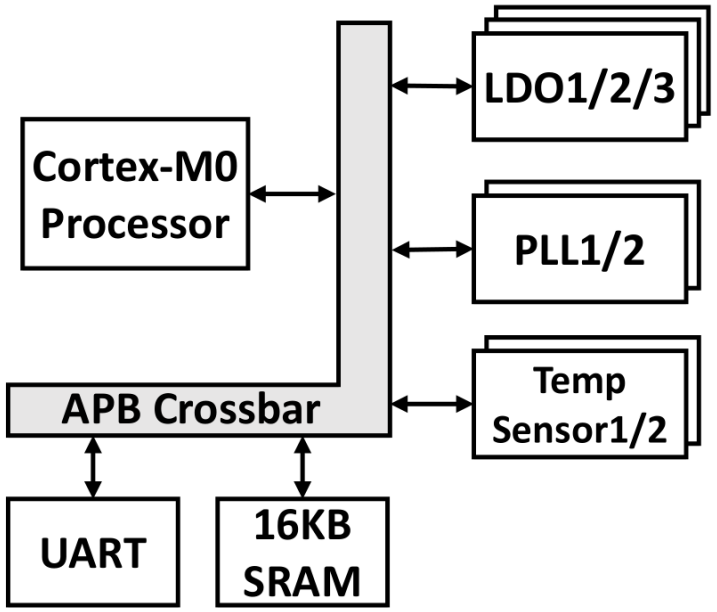
- **Input Specifications**
  - Depth/Capacity
  - Word size
  - Operating voltage
  - Operating frequency

- **Generator Results**
  - Normalized energy and delay plots for various memory sizes while sweeping VDD for 8KB Memory

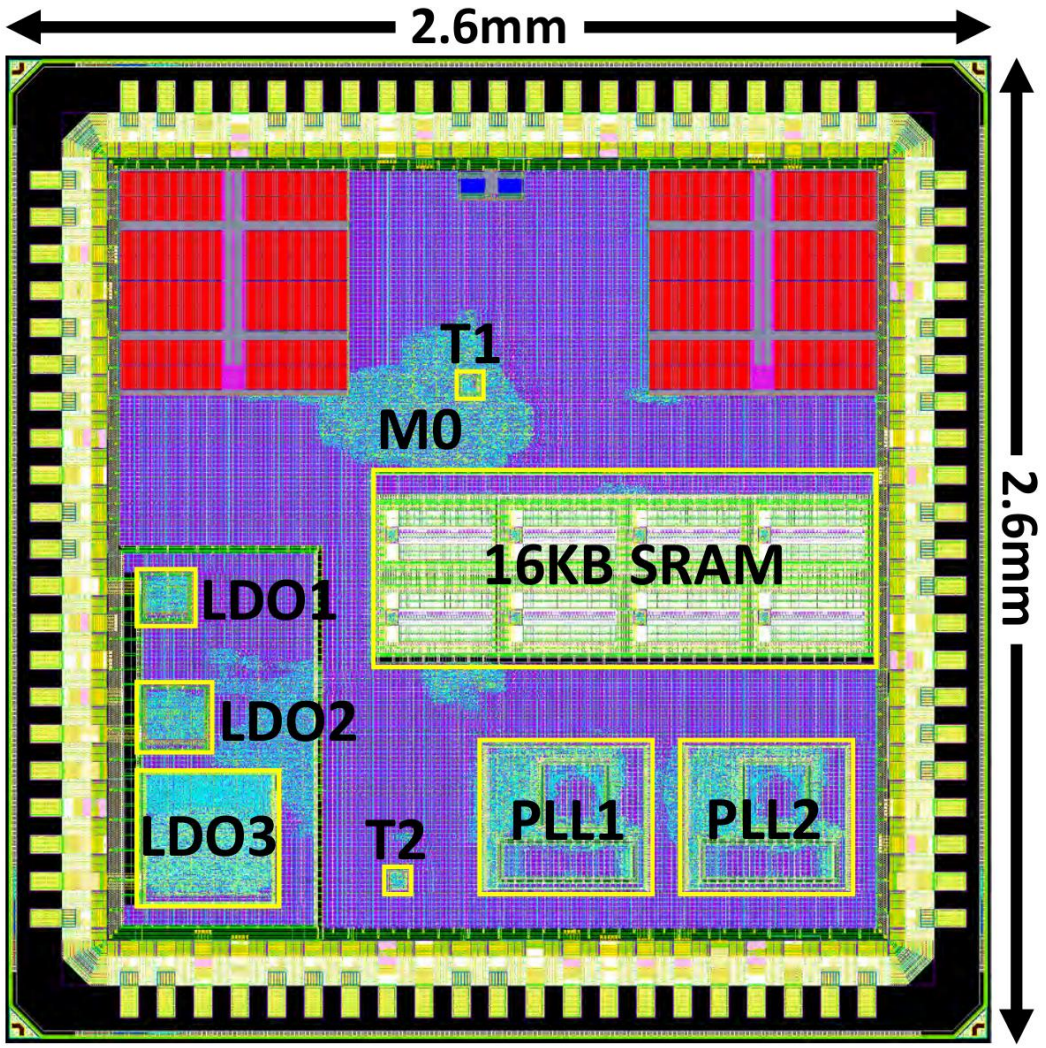


Prototype Evaluation: Chip Prototype

- **Chip Details**
  - 65nm Process
  - 2.6 x 2.6mm
- **Block Diagram**



- **Annotated Die Photo**



Conclusion

- FASoC is a fully autonomous framework to generate completely integrated SoC designs based on user input specifications
- The framework is PDK-agnostic and EDA tool flexible
- The framework includes generators for PLL, LDO, temperature sensor and SRAM blocks
- Delivers faster turn-around times when building custom analog blocks and integrating them into larger SoC designs
- Prototype SoC created in a 65nm process with validated silicon results

ACKNOWLEDGMENT

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