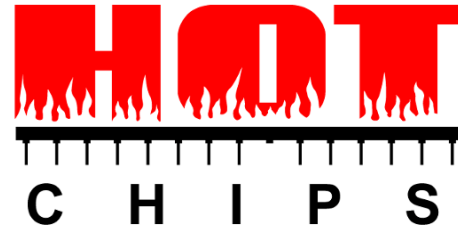
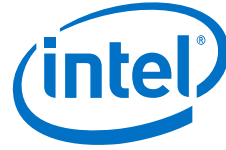


HOT
C H I P S



Inside Tiger Lake: Intel's Next Generation Mobile Client CPU

Xavier Vera

Principal Engineer, Client Performance Architecture
Intel Corporation

Tiger Lake Architecture

Goals

CPU

Greater than generational performance in CPU

GPU

Disruptive performance in integrated graphics

AI

Scalable AI for emerging client workloads



Increased memory & fabric efficiency for high bandwidth



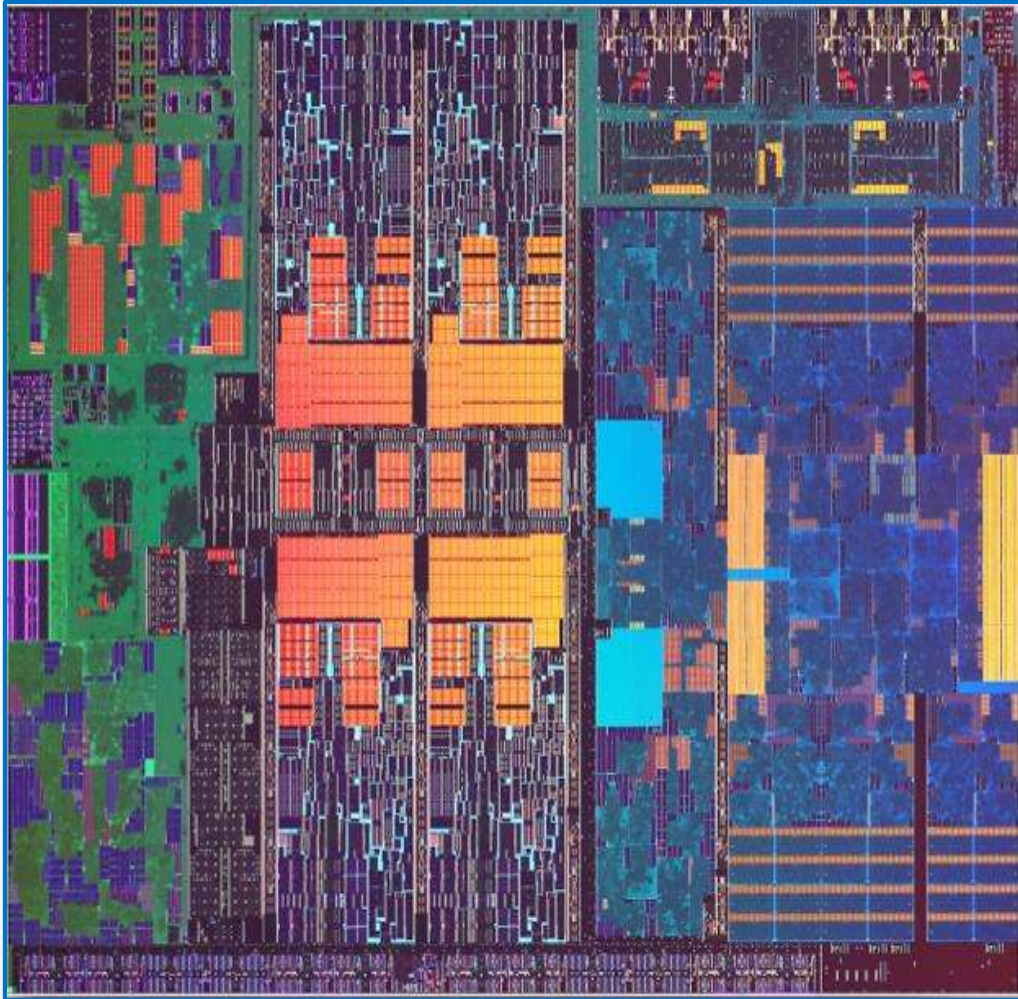
Best in class set of IPs throughout the SoC



Continue to advance Intel's SoC Security

.... all at the same power envelopes with increased power efficiency

Outline



Intel 10nm SuperFin Process Technology

SoC Architecture

Willow Cove Core

X^e Graphics

SoC Uncore, IO and Display

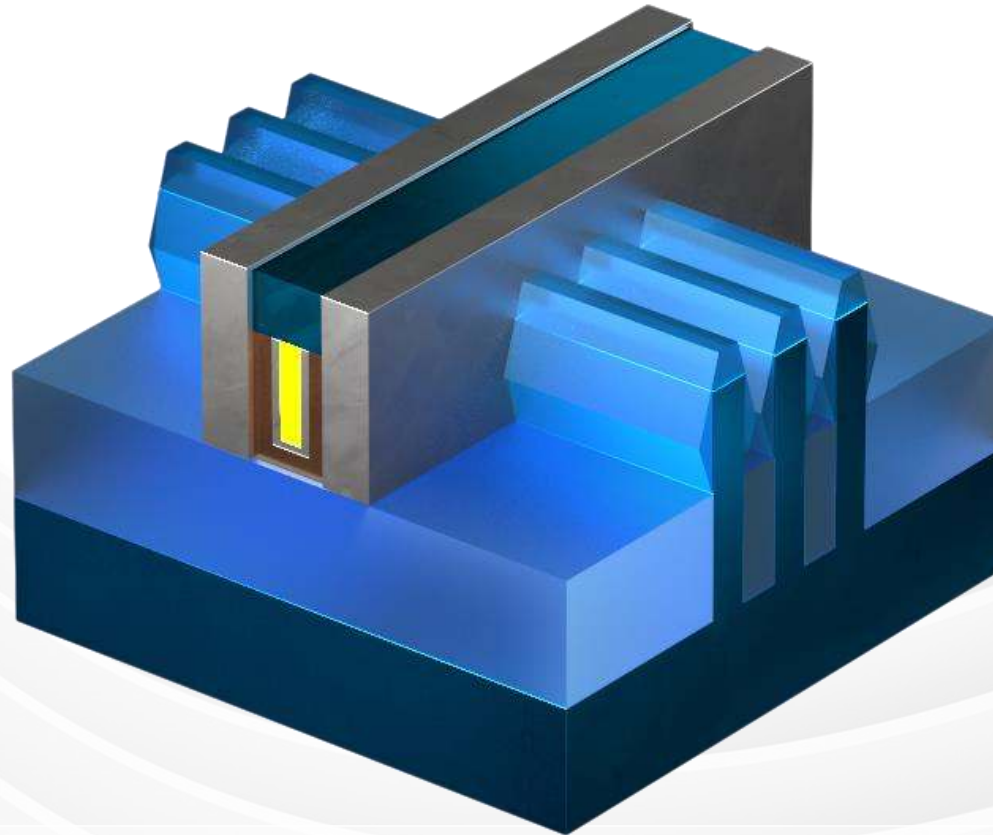
Power Management

New High Performance XTOR

Innovation Across The Entire Stack, From Channel To Interconnects

Additional Gate Pitch
Higher Drive Current

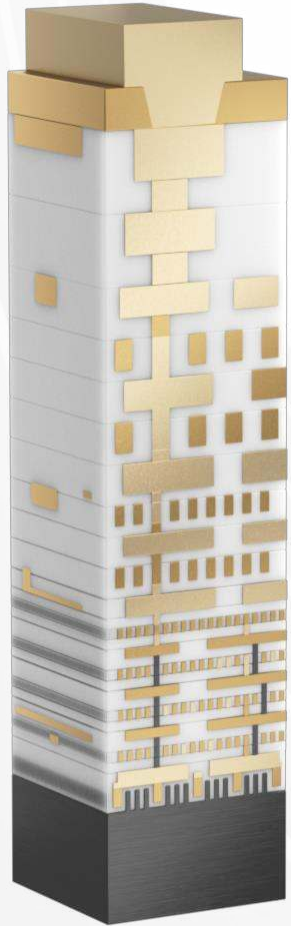
Improved Gate Process
Higher Channel Mobility



Enhanced Epitaxial Source/Drain
Lower Resistance, Increases Strain

Improved Metal Stack

Innovation Across The Entire Process Stack, From Channel To Interconnects



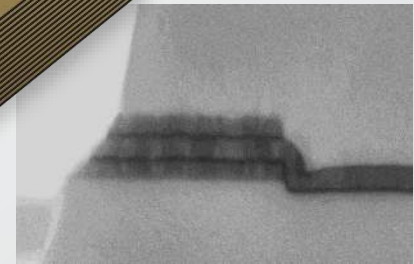
Super MIM Capacitor

>5x increase in MIM capacitance

Novel Thin Barrier

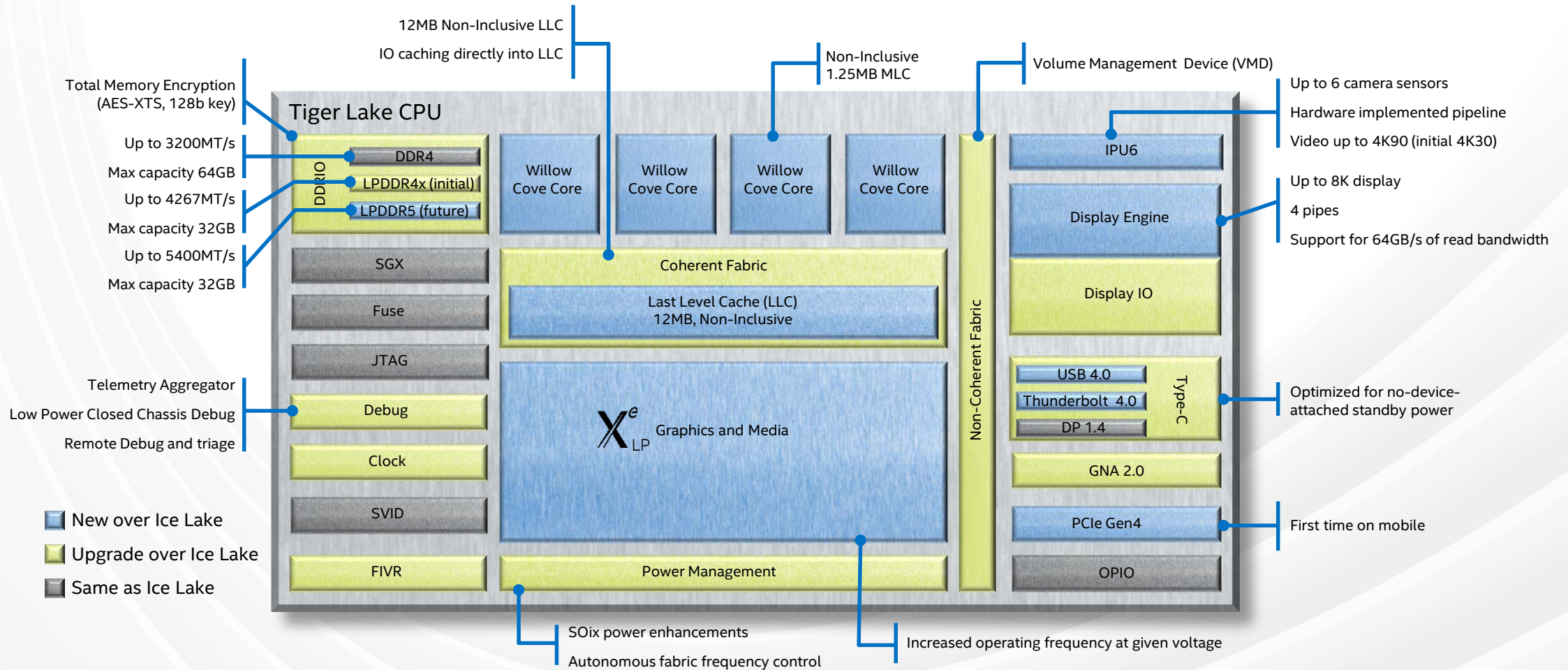
reduces via resistance by 30%

Thin layers of different Hi-K materials, each just a few Angstroms thick, stacked in a repeating "superlattice."



Architecture and Design Improvements

Introducing Tiger Lake

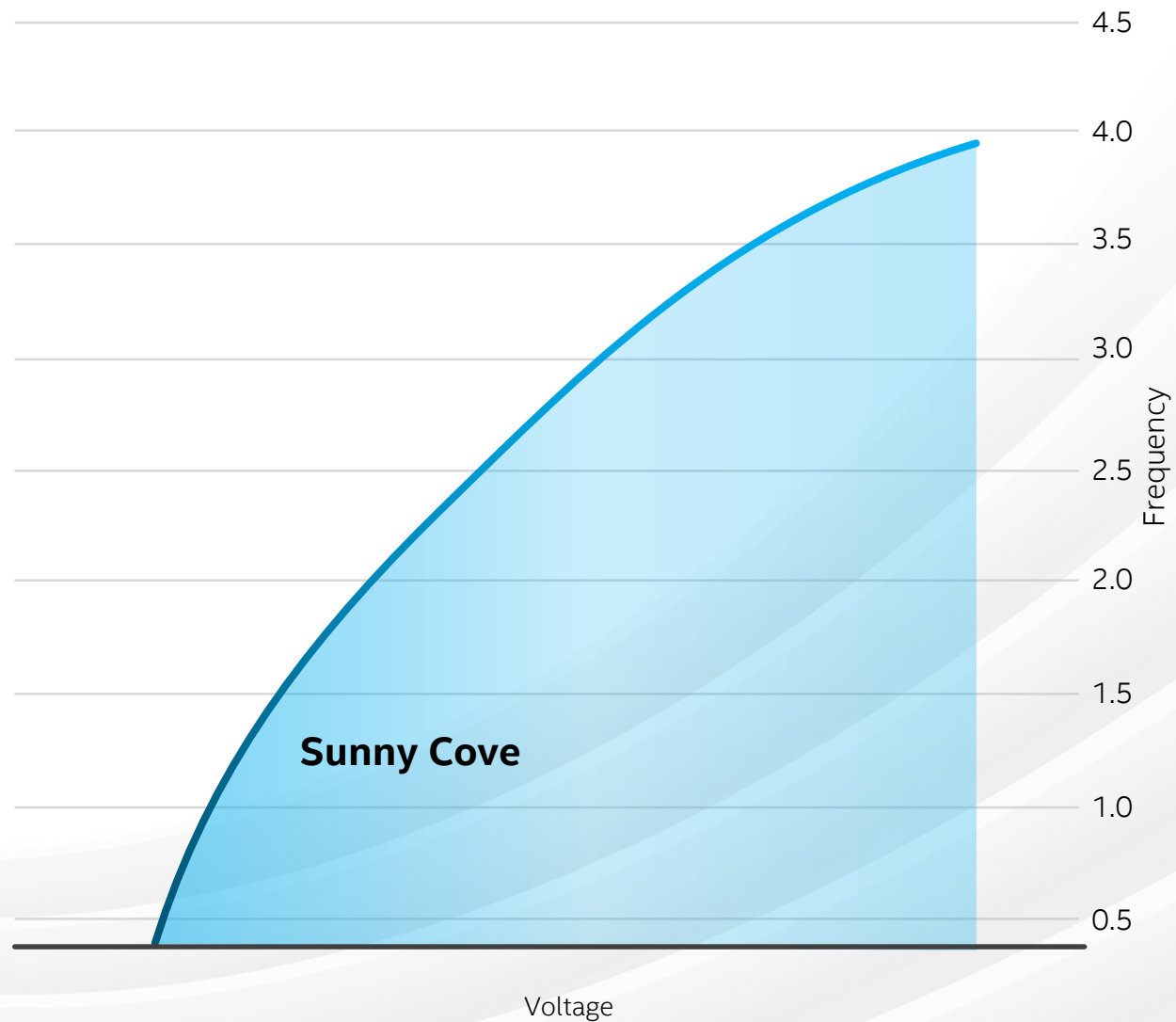


Willow Cove Core



- Built on the Sunny Cove architectural foundation
- Redesigned fundamental circuits to take advantage of SuperFin technology
- Redesigned caching architecture to larger non-inclusive, 1.25MB MLC
- Control Flow Enforcement technology to help protect against return/jump oriented attacks

The Result



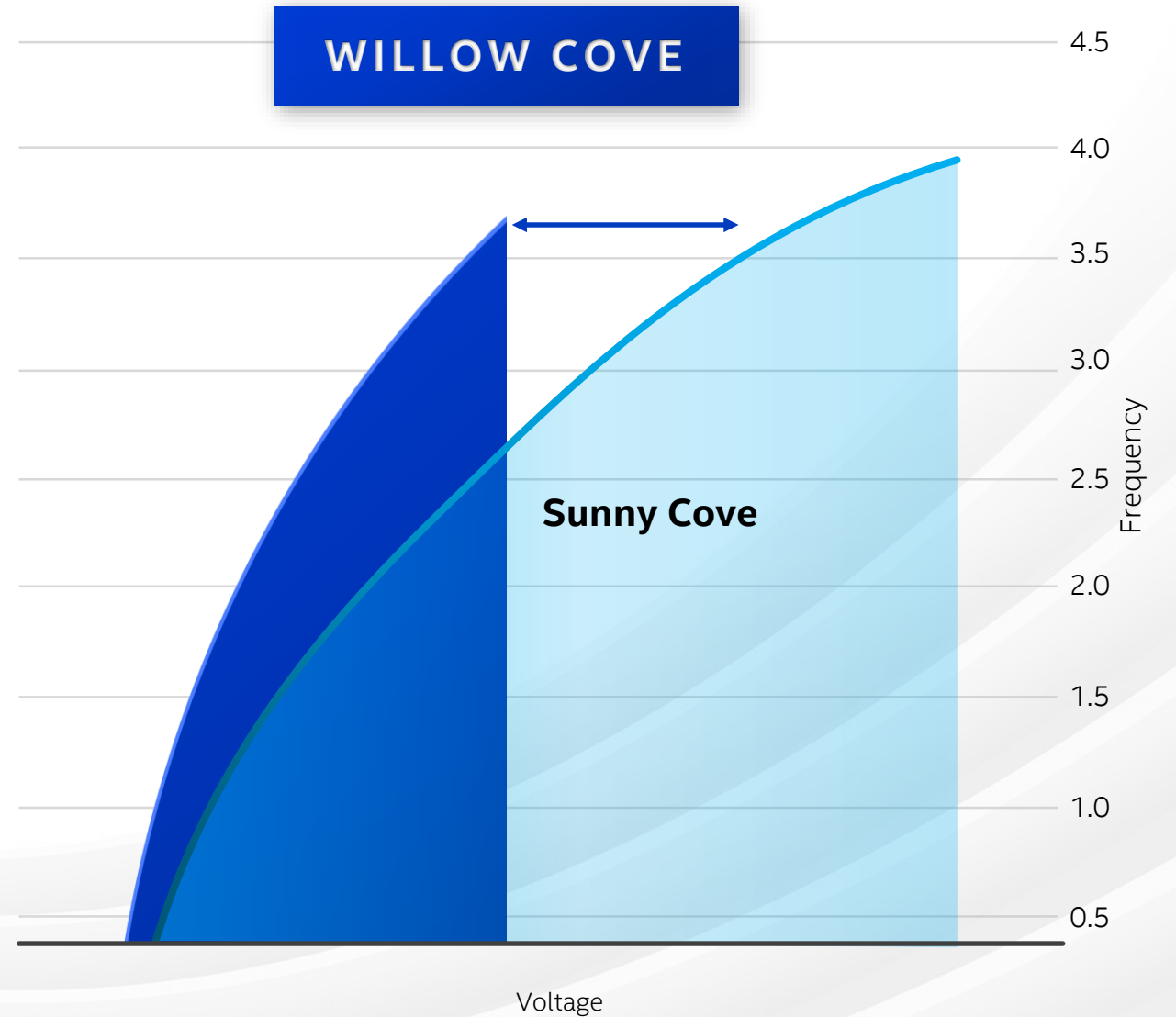
The Result

Large Frequency Gains



The Result

Increased Power Efficiency



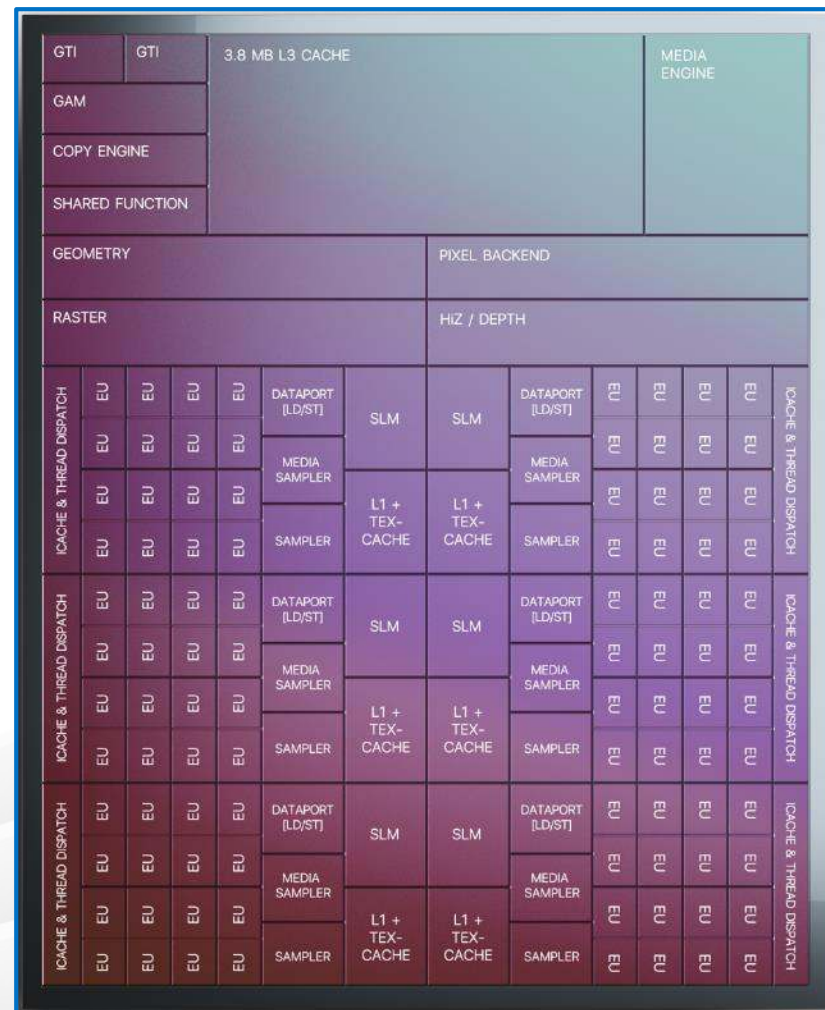
The Result

Greater Dynamic Range



X^e_{LP} Graphics

- Large improvements in performance per watt efficiency
- Up to 96EUs with increased capabilities
- 3.8MB L3 cache
- Increased bandwidth to LLC and Memory



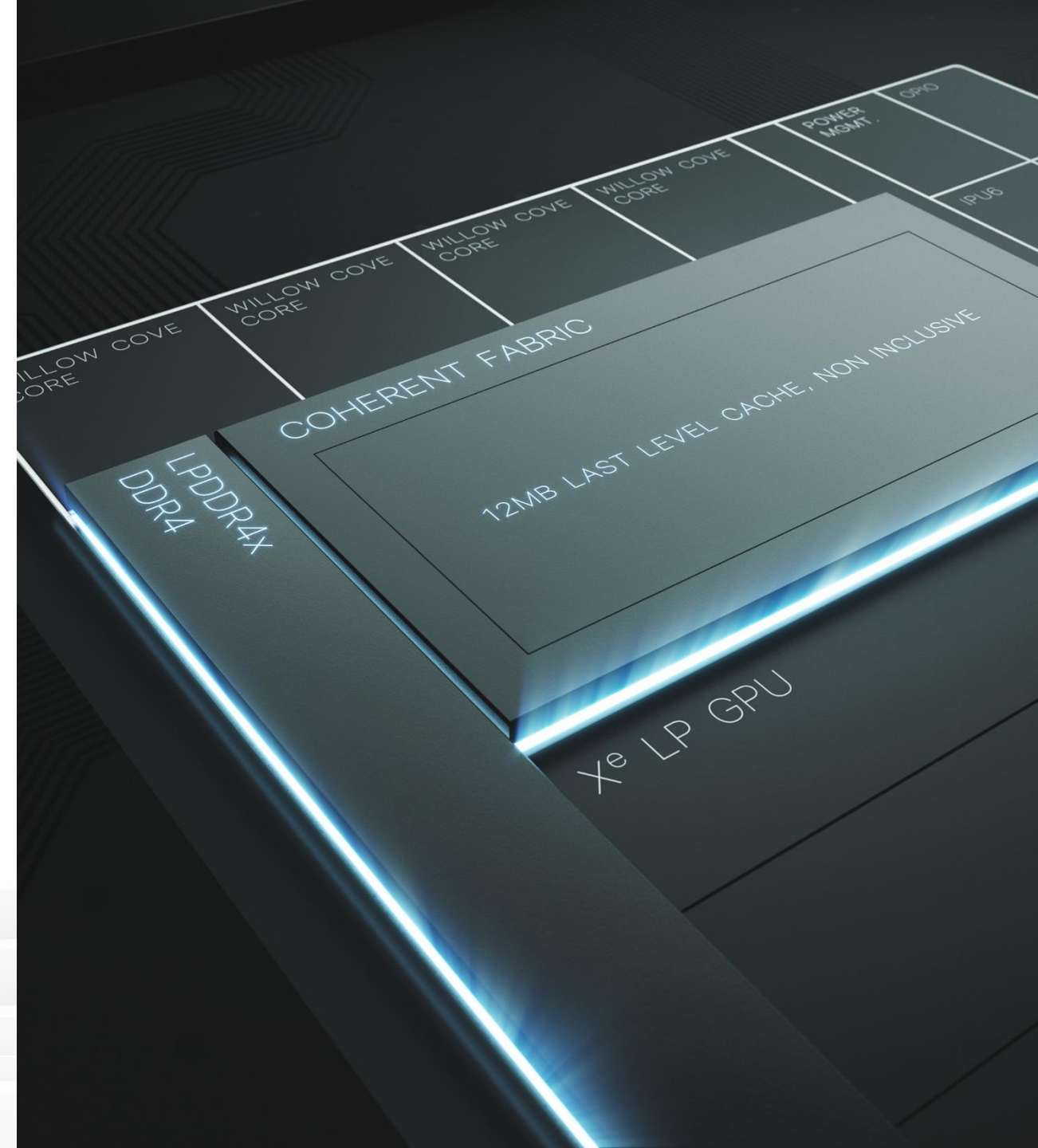
Fabrics and Memory

Coherent Fabric

- 2x increase in coherent fabric bandwidth
 - Dual ring microarchitecture
- 50% LLC size increase to non-inclusive
- IO caching

Memory

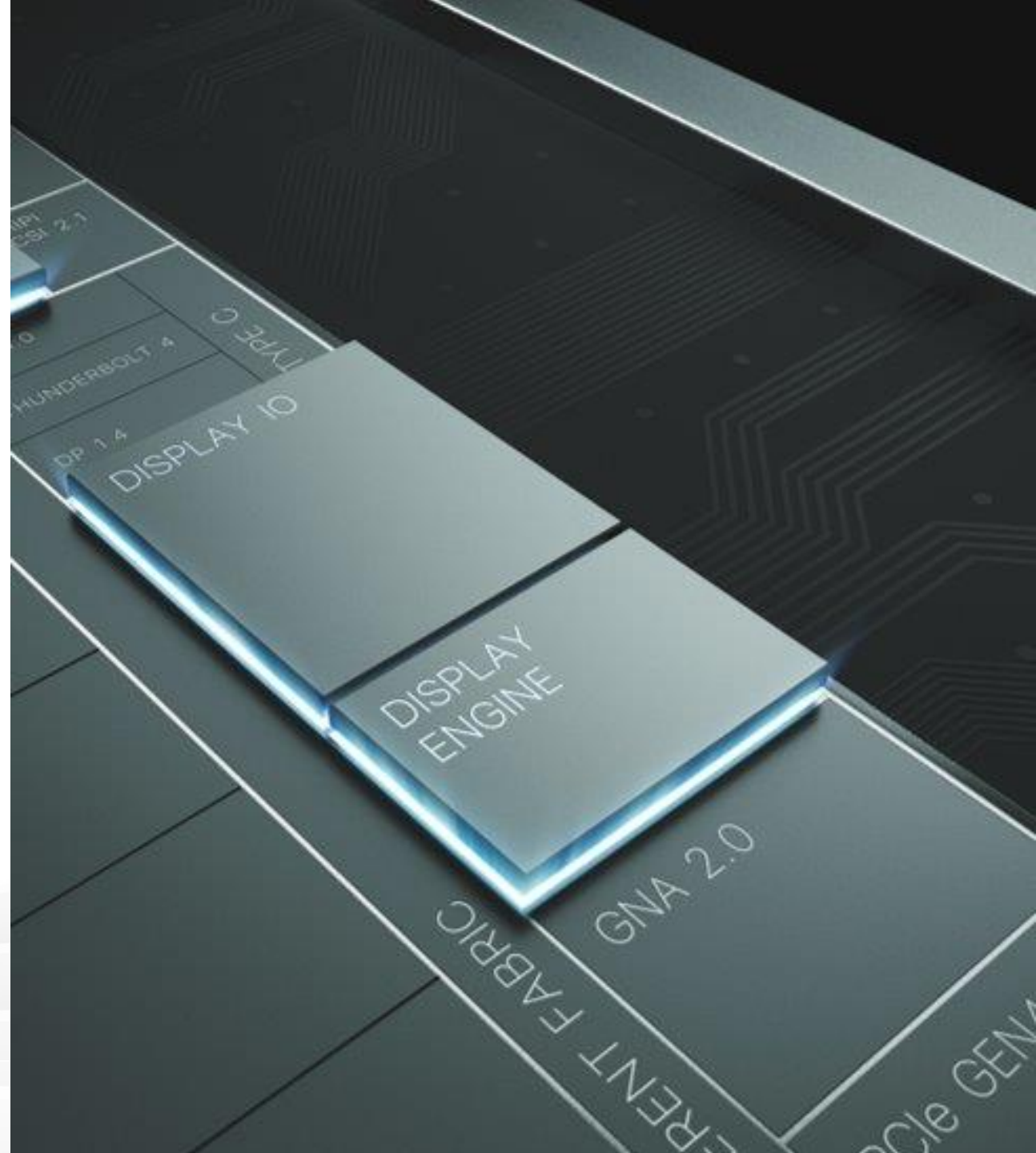
- More efficient memory bandwidth for graphics and cores
 - Support for up to ~86GB/s of memory bandwidth
 - Deeper, narrower dual memory controller for higher efficiency
- Architectural support for LP4x-4267 and DDR4-3200 (initial) and up to LP5-5400
- Intel® Total Memory Encryption



Display

Connectivity

- The future calls for more displays, higher resolutions and better image quality
 - 8K displays
- Added a dedicated fabric path (DIP) to memory to maintain quality of service
 - Up to 64GB/s of isoch bandwidth
- External display connectivity through DP/HDMI protocols



IO

PCIe Gen4 on CPU for low latency, high bandwidth device access to memory

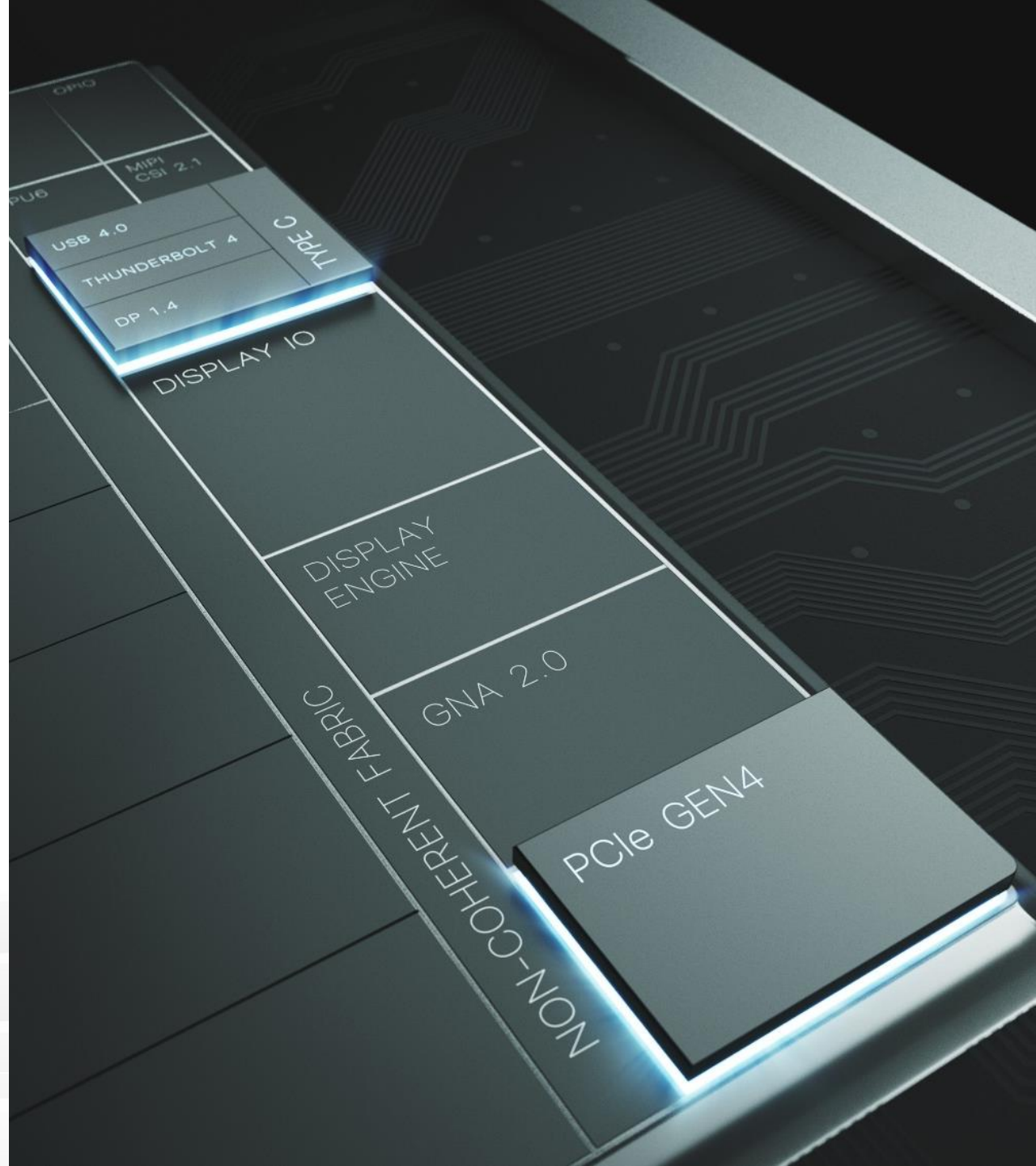
- Full 8GB/s bandwidth to memory
- ~100ns less latency when attached to CPU vs PCH

Integrated Thunderbolt 4 and USB4 support

- Up to 40Gb/s bandwidth on each port
- USB tunneling

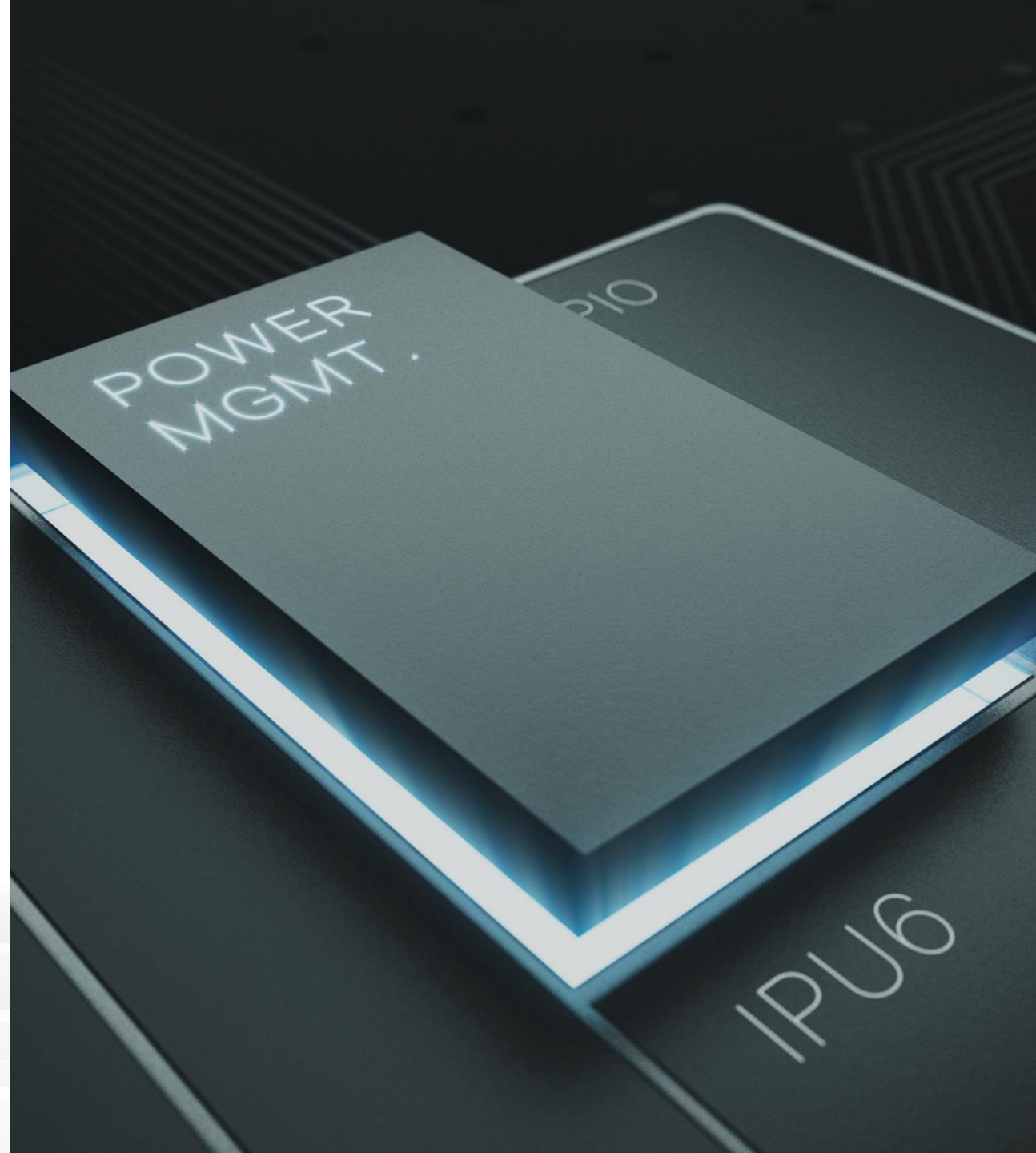
Integrated Display output via Type-C

- DP alternate mode/tunneling over Thunderbolt
- DP-in ports for discrete graphics card display output to mux over type-C port
- HDMI/DP/Type-C connectors supported



Power Management

- Moved extensive logic to gated power domains
- Increased FIVR efficiency
- Deeper package C state turning off all clocks in CPU
- Hardware-based save and restore logic
- Autonomous DVFS in coherent fabric and memory subsystem to optimize frequency and voltage based on bandwidth and latency



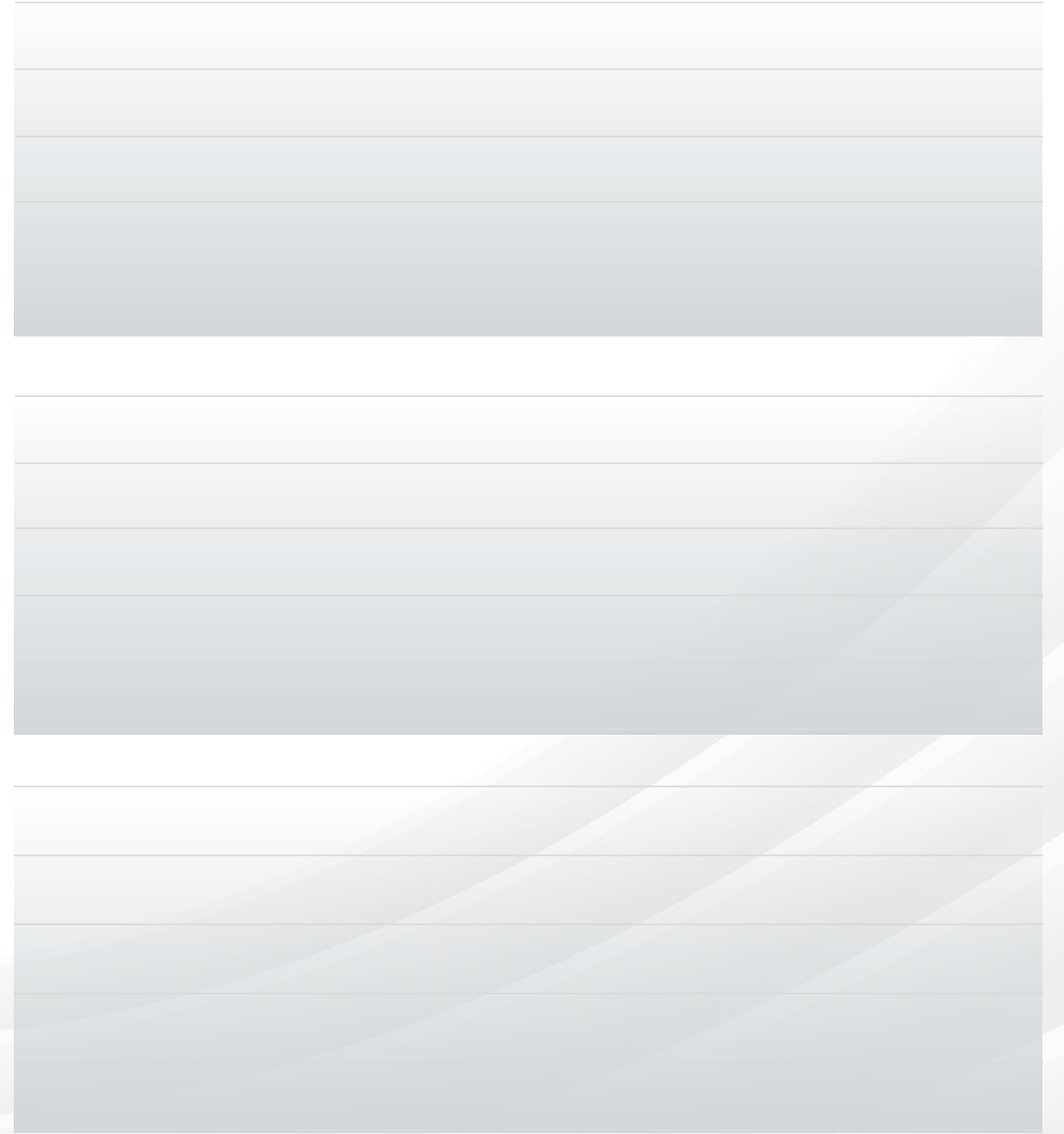
PM - DVFS

- Goal is to adapt frequencies (and voltages) to required performance level

CORE

FABRIC

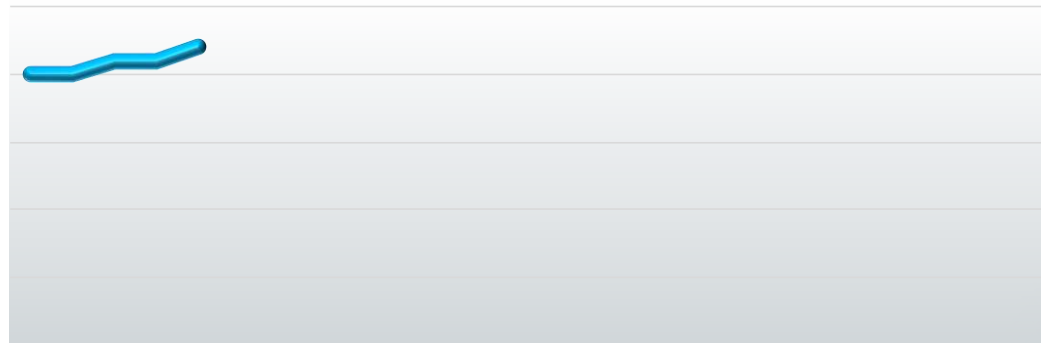
MEMORY



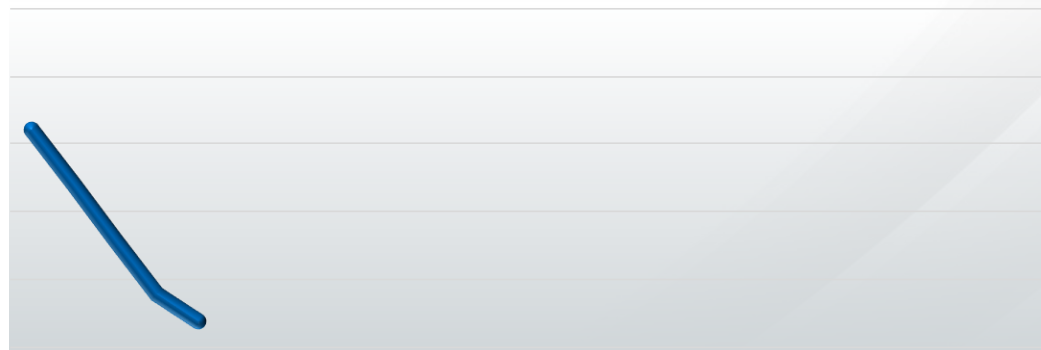
PM - DVFS

- Workload is in a core centric phase with few requests
- Core increases frequency to match required performance
- Fabric and memory reduce frequency to match low number of requests

CORE



FABRIC



MEMORY



PM - DVFS

- Workload enters a phase where requests go out to fabric and hit the large LLC
- Core reduces the frequency, while fabric increases it to match the increasing number of requests
- Memory stays at low frequency since requests are served from cache

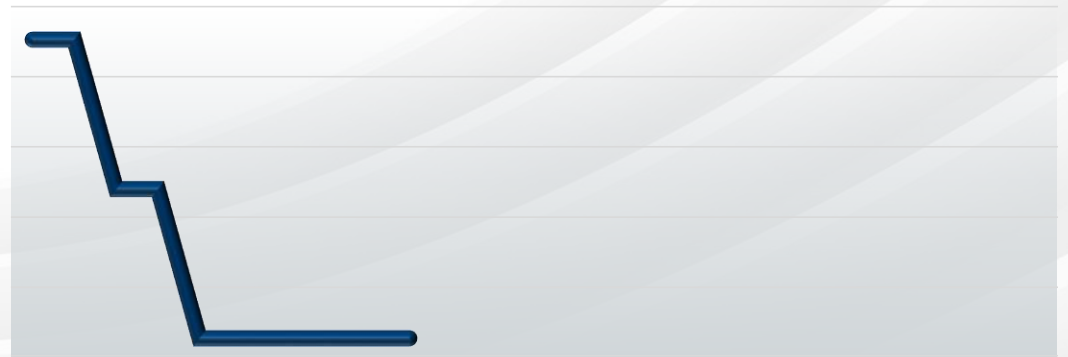
CORE



FABRIC



MEMORY



PM - DVFS

- Workload enters a phase where data requests miss in the LLC and go to memory
- Core keeps reducing frequency
- Memory increases frequency to match the increasing demand
- Fabric can reduce frequency

CORE



FABRIC



MEMORY



PM - DVFS

- Working set is within the core caches, core raises the frequency to deliver max frequency, while fabric and memory stay at the minimum frequency to deliver the few requests

CORE



FABRIC



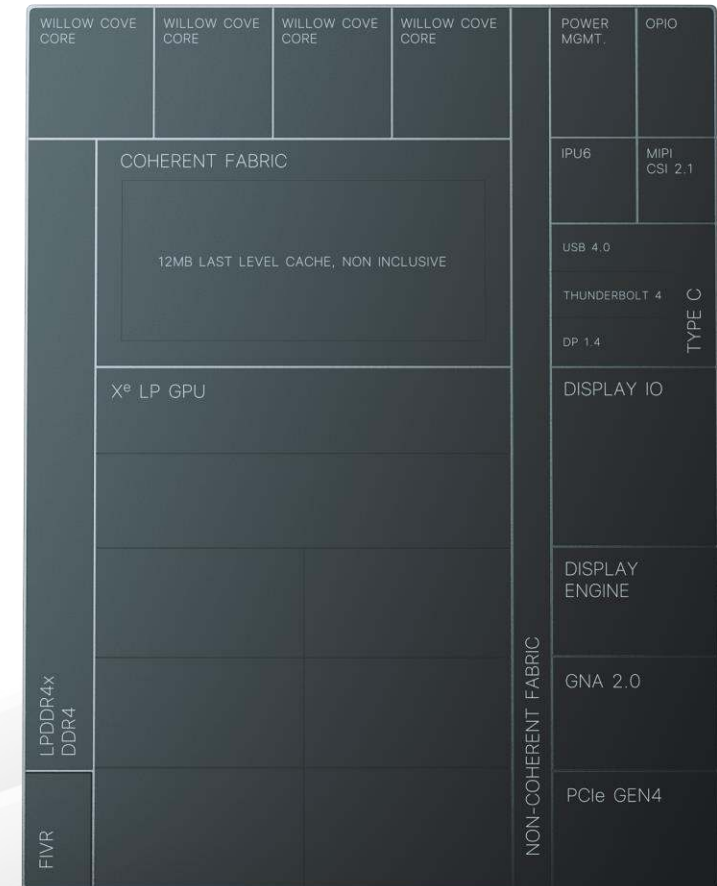
MEMORY



Tiger Lake SoC Architecture

Leveraging Process Tech Improvements, Tiger Lake SoC Architecture delivers significant advancements across a wide set of SoC IPs, with:

- More than a generational increase in CPU performance in Willow Cove CPU core
- Massive improvements in graphics power efficiency in Xe^e-LP graphics IP
- Improved fabric and memory to deliver more bandwidth *efficiently*
- Rich I/O... and much more!



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Capacitance and resistance measurements and CPU utilization rates are based on silicon projections and preliminary development board measurements as of March 2020. They may not reflect all publicly available updates and are subject to change.

Software and workloads used in performance tests may have been optimized for performance only on Intel microprocessors.

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