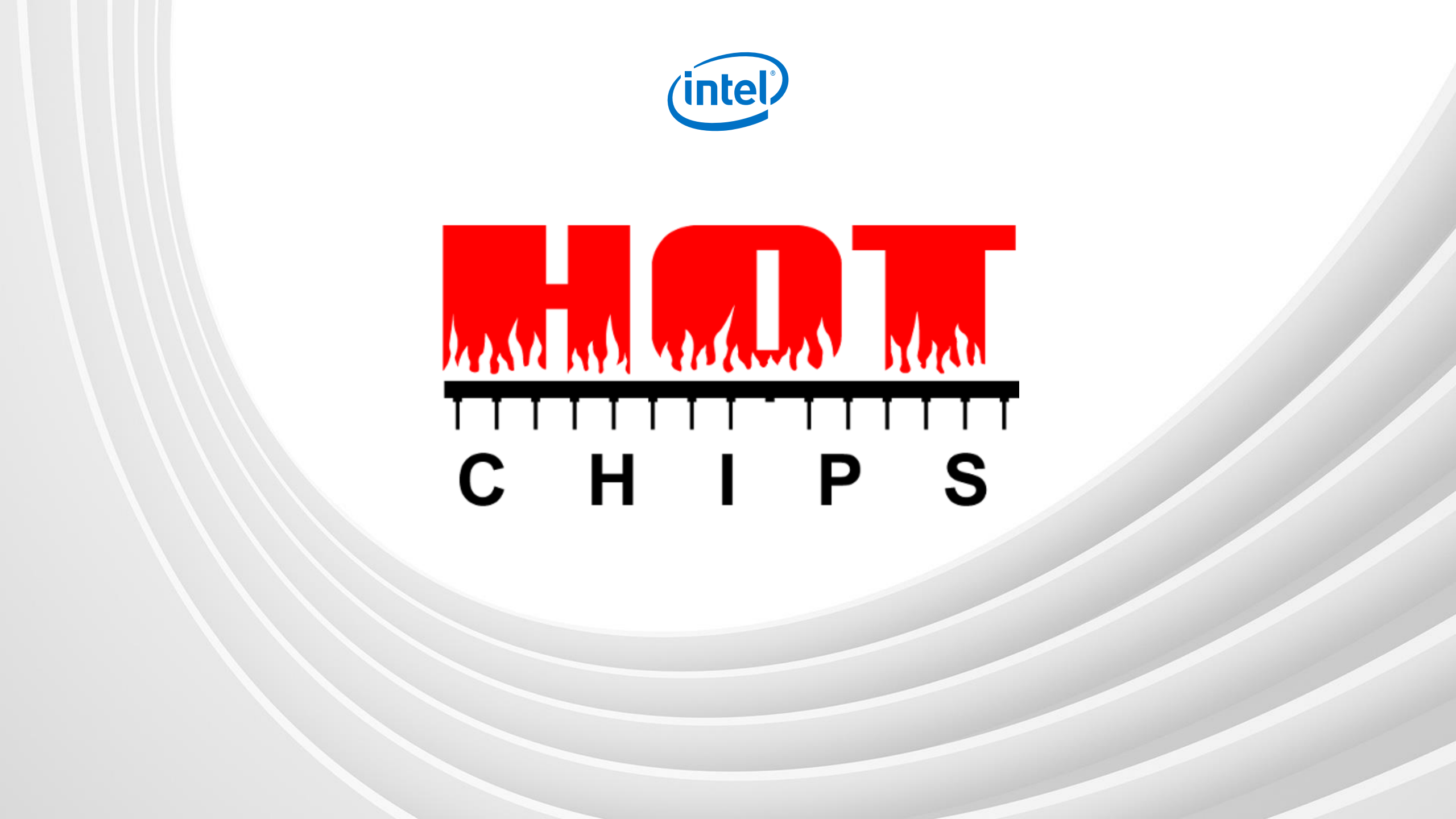
intel
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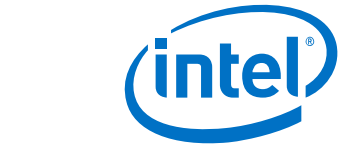
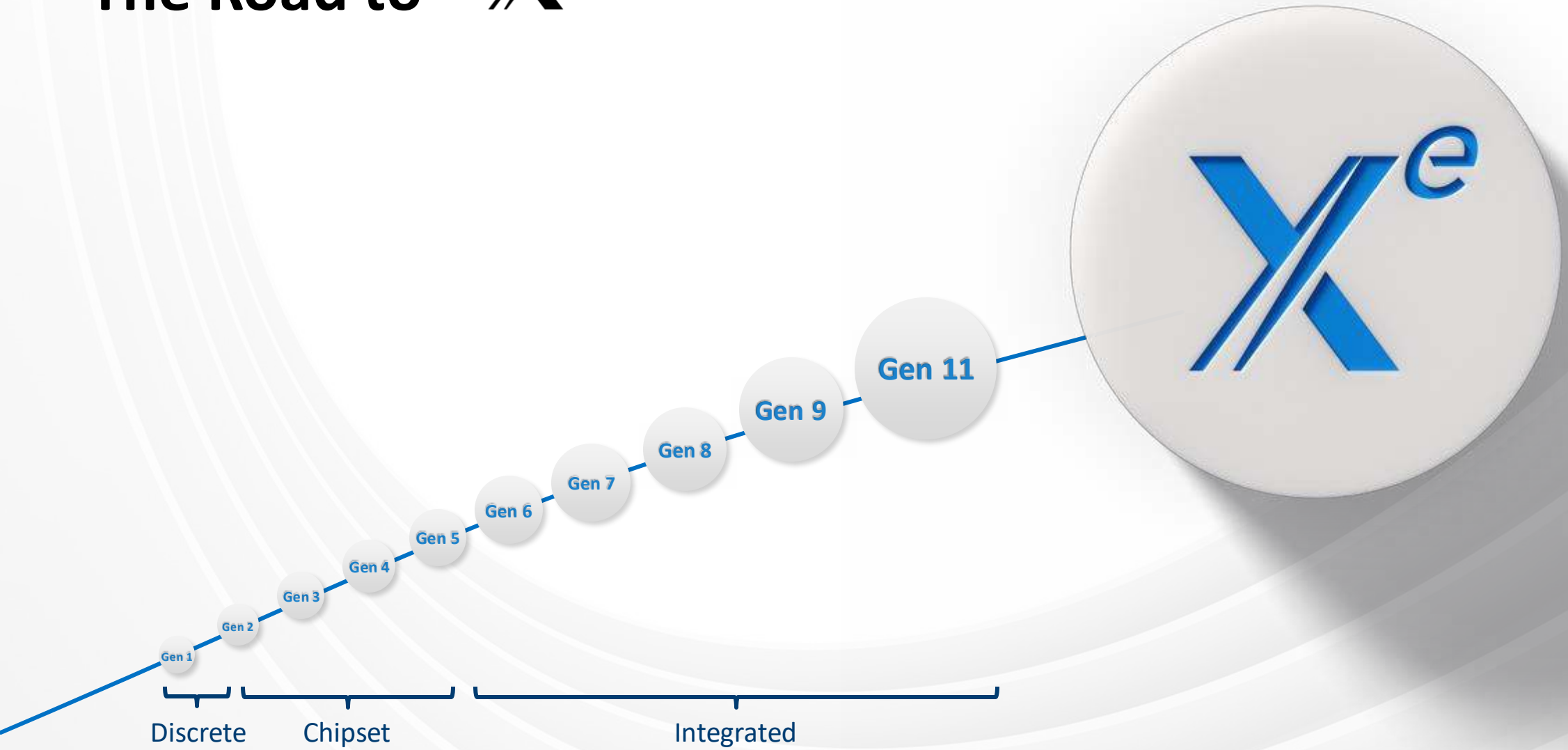
CHIPS



The Xe GPU Architecture

David Blythe
Chief GPU Architect, Intel Corporation

The Road to Xe



Architecture Goals

SCALABILITY & CONFIGURABILITY

NEW CAPABILITIES

POWER, PERFORMANCE & AREA

Intel GPU Architecture

One Architecture and 4 Micro Architectures

Xe HPC — HPC EXASCALE

Xe HP — DATA CENTER / AI

ENTHUSIAST

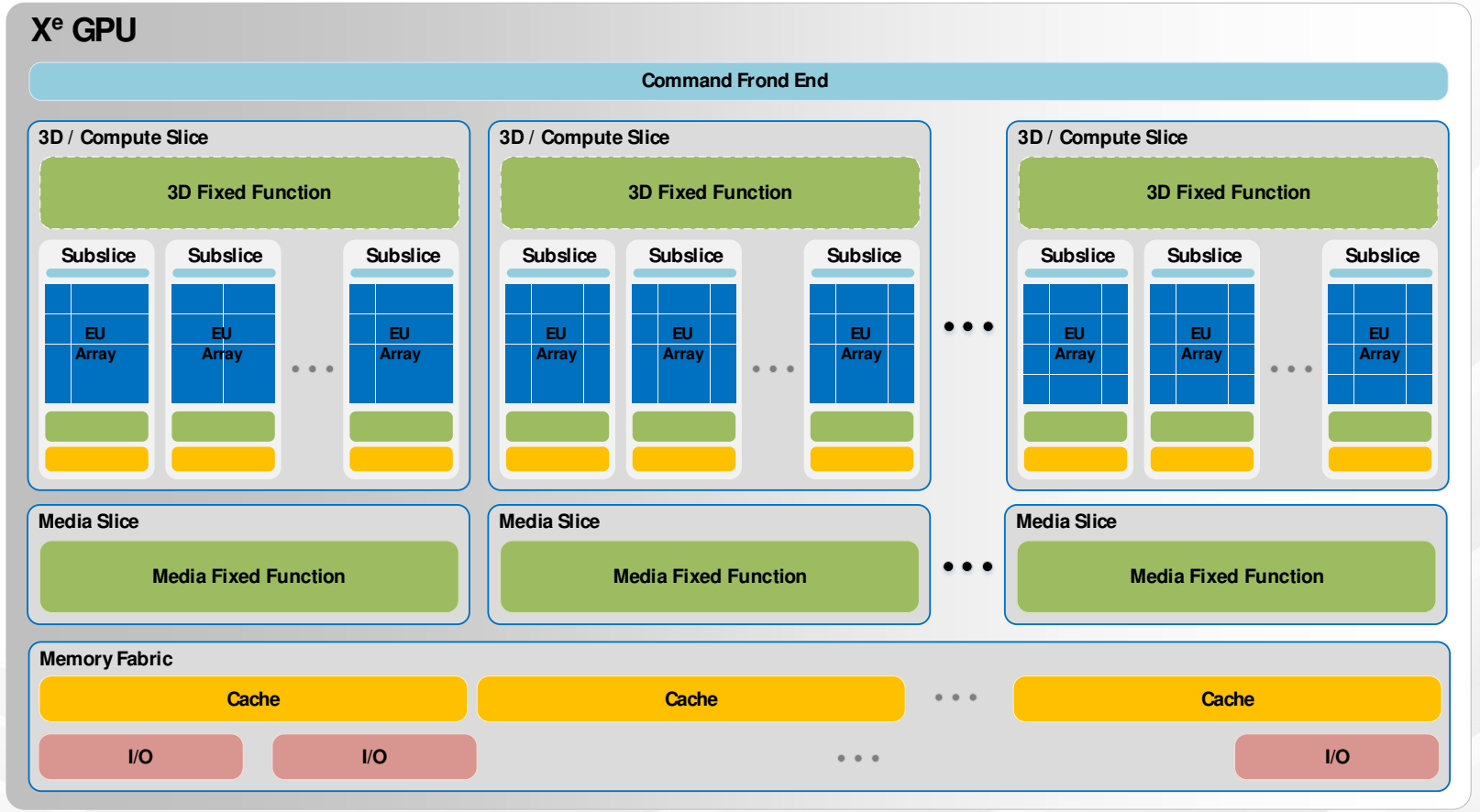
Xe HPG — MID RANGE

Xe LP — INTEGRATED + ENTRY

Teraflops to Petaflops

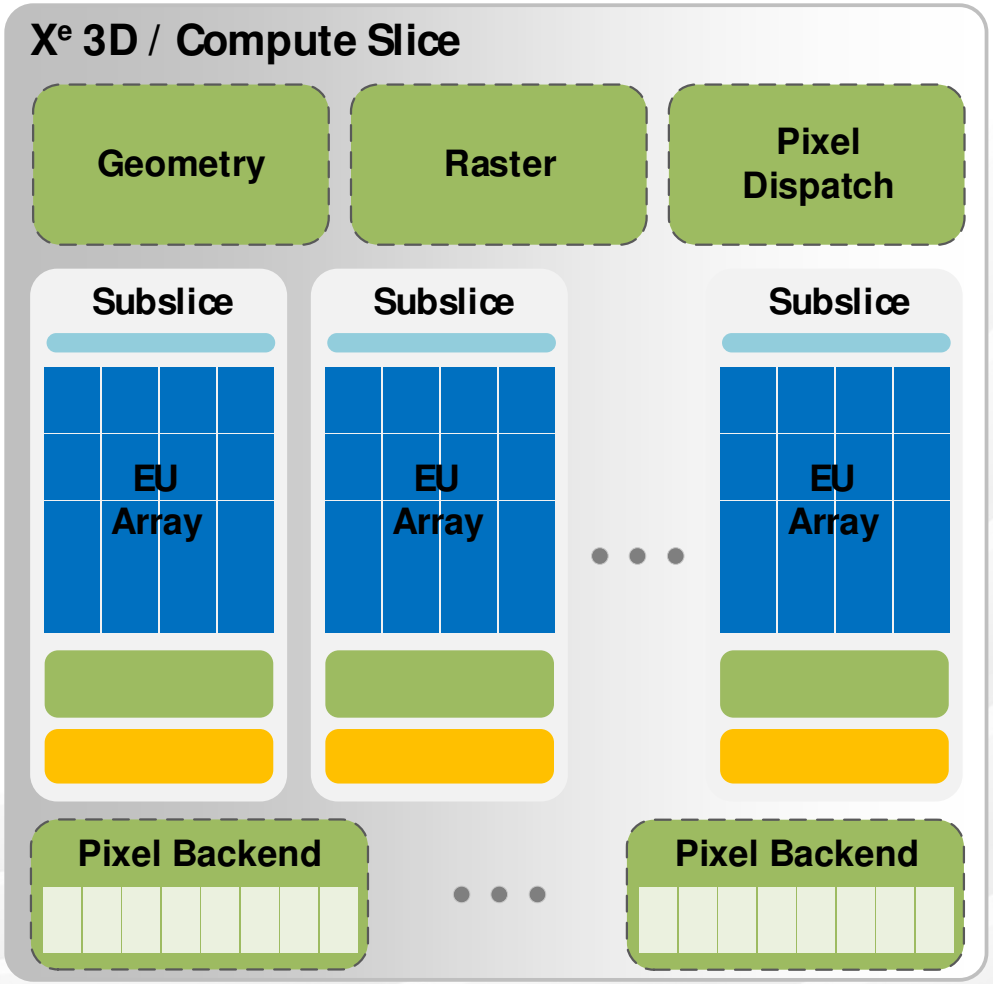
High Level Xe Architecture

- 3D / Compute Slice
- Media Slice
- Memory Fabric / Cache



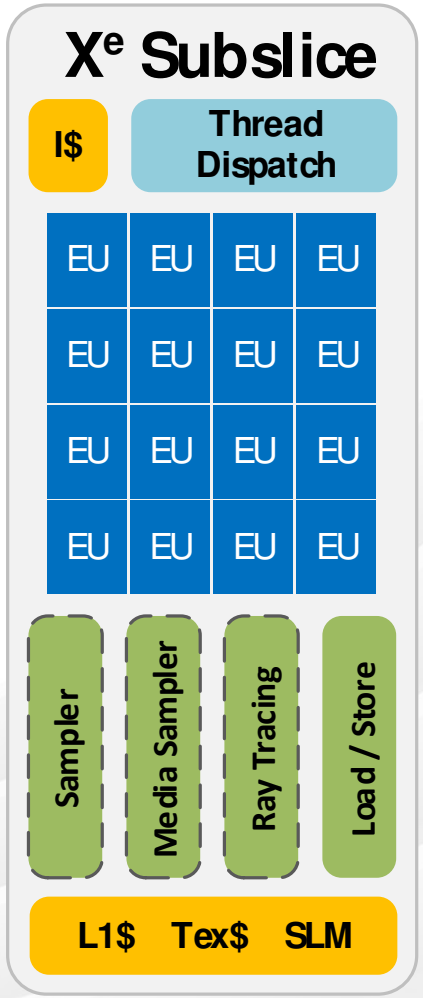
Xe 3D/Compute Slice

- Variable number of Subslices
- 3D Fixed Function **(optional)**
  - Geometry
  - Setup and Raster
  - Color, Z, HiZ



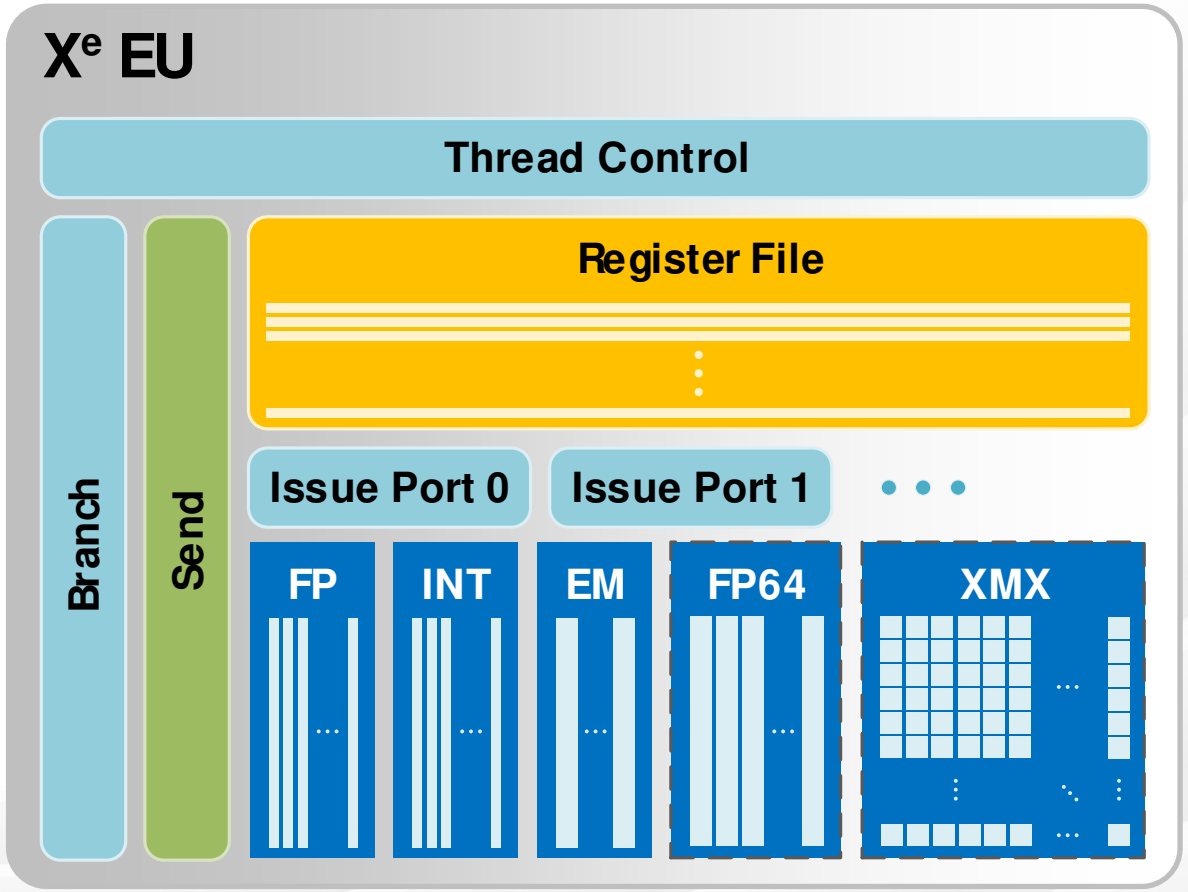
Xe Subslice

- 16 EUs
- Thread dispatch
- Instruction cache
- L1, texture cache and shared local memory
- Load / Store
- Fixed Function **(optional)**
  - 3D sampler
  - Media sampler
  - Ray Tracing



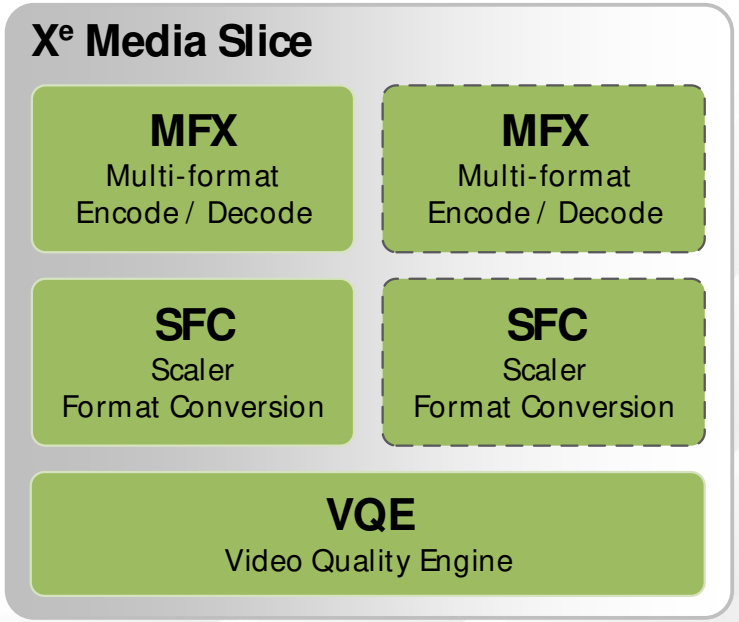
Xe Execution Unit

- Thread control
- Register file
- Branch
- Send
- Multiple issue ports
- Configurable mapping of vector pipes
  - Floating Point
  - Integer
  - Extended Math
  - FP64 **(optional)**
  - Matrix Extension (XMX) **(optional)**



Xe Media Slice

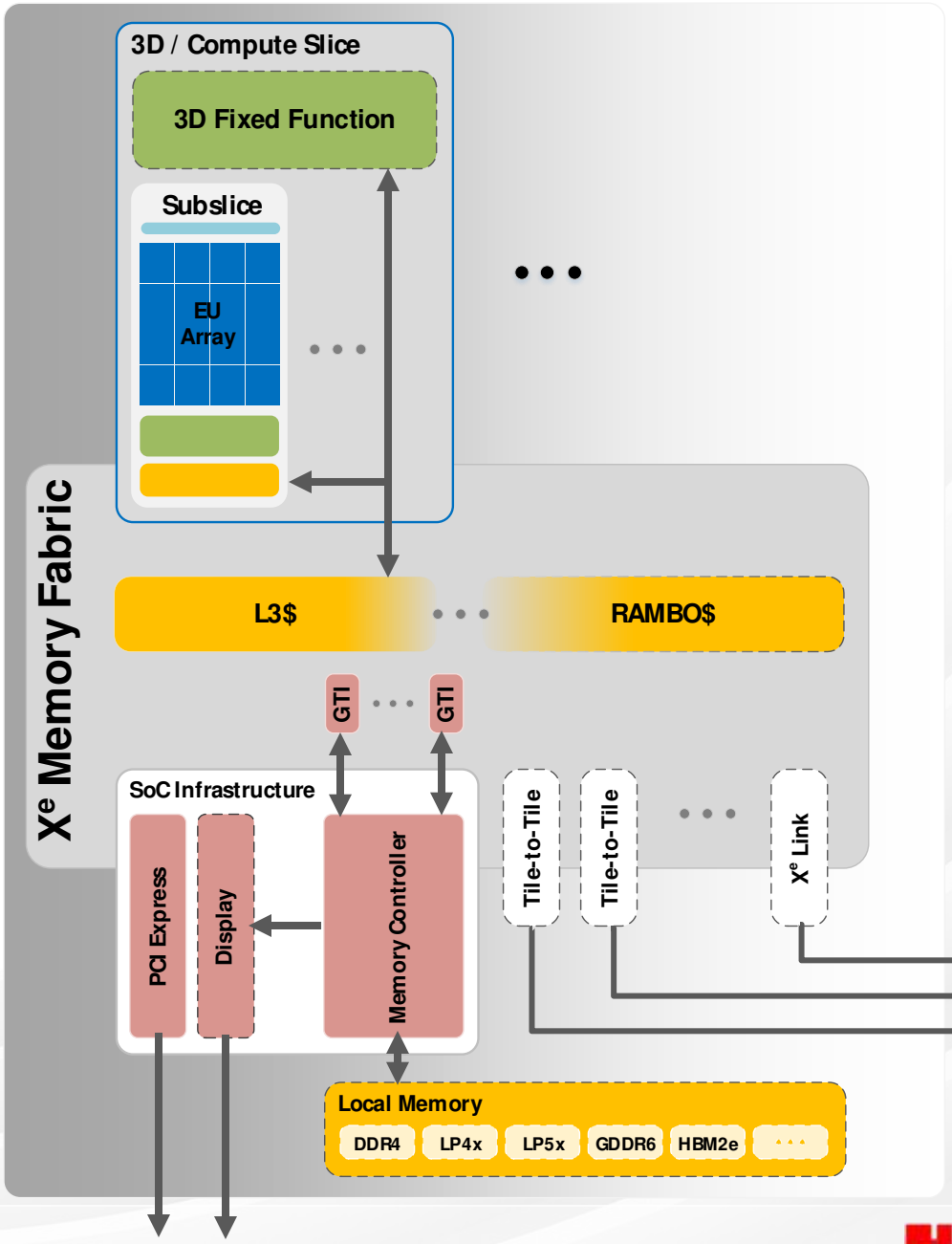
- Media slices are independent
- Software can distribute a high-resolution stream across multiple slices
- Fixed function units:
  - MFX - encode / decode / transcode
  - SFC - scaling and format conversion
  - VQE - video quality engine



Xe Memory Fabric

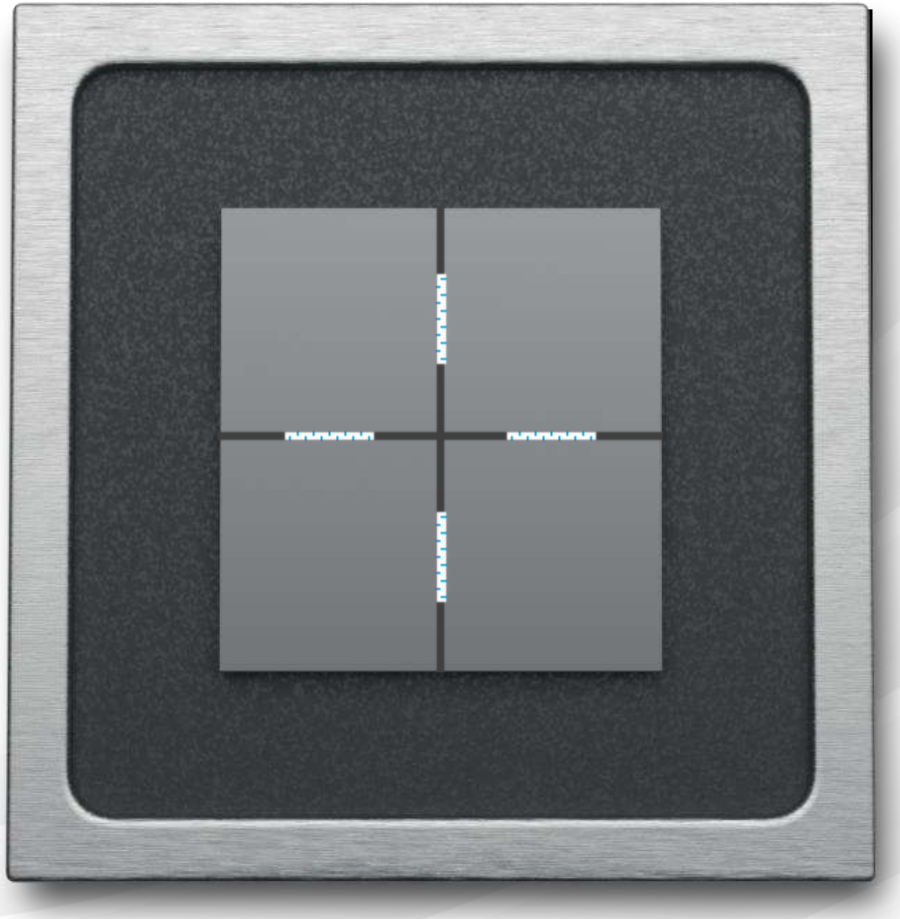
Coherent Scalable Interconnect Fabric

- Slices
- L3 + Rambo **(optional)**
- SoC infrastructure
  - PCIe
  - Display **(optional)**
  - Memory Controller
    - Local Memory **(optional)**
- Extendable **(optional)**



Intra-Package Scaling

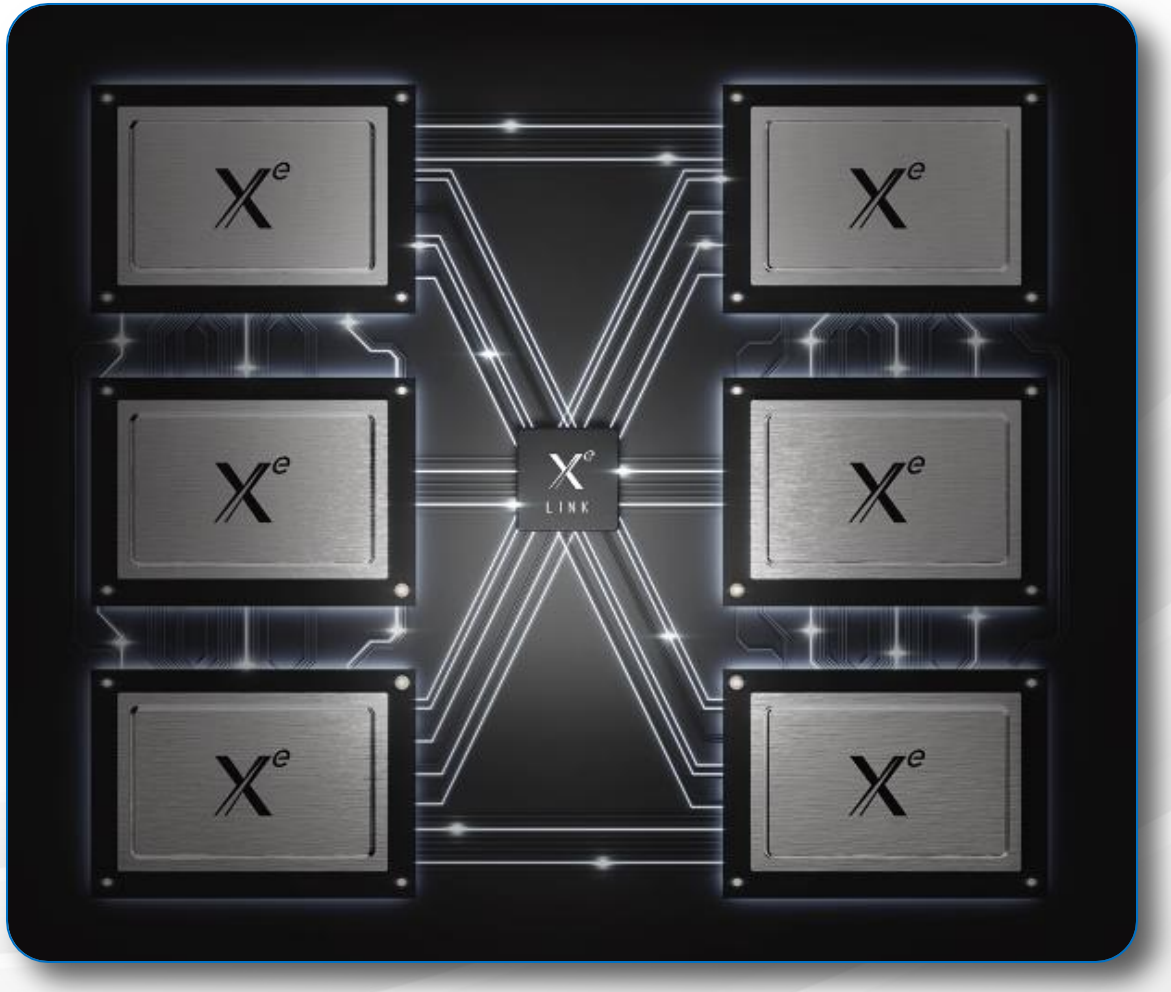
- X^e instantiated as a tile
- EMIB bridges interconnect tiles over X^eMF
- Package-time option to integrate up to 4 tiles



Multi-tile GPU

Inter-Package Scaling

- X^e Link for system level scalability
- Connect through X^eMF
- X^e_{HPC} implementation: I/O tiles and EMIB



Micro-architectures

Xe LP	Xe HPG	Xe HP	Xe HPC
Low Power Optimized	**Discrete Gaming Optimized**	**Machine Learning & Media Optimized**	**HPC & Machine Learning Optimized**
Single slice design Integrated and discrete …	GDDR6 memory Ray tracing …	1-4 tiles per package HBM2e memory …	1-2 tiles per package HBM2e memory Xe Link interconnect Co-EMIB (Foveros + EMIB) …
In production	**In the lab**	**In the lab**	**In fabrication**
Tiger Lake DG1 SG1	TBD	TBD	Ponte Vecchio

PRODUCTS

TIGERLAKE
LEADERSHIP INTEGRATED GRAPHICS

DG1
GPU FOR MOBILE CREATORS

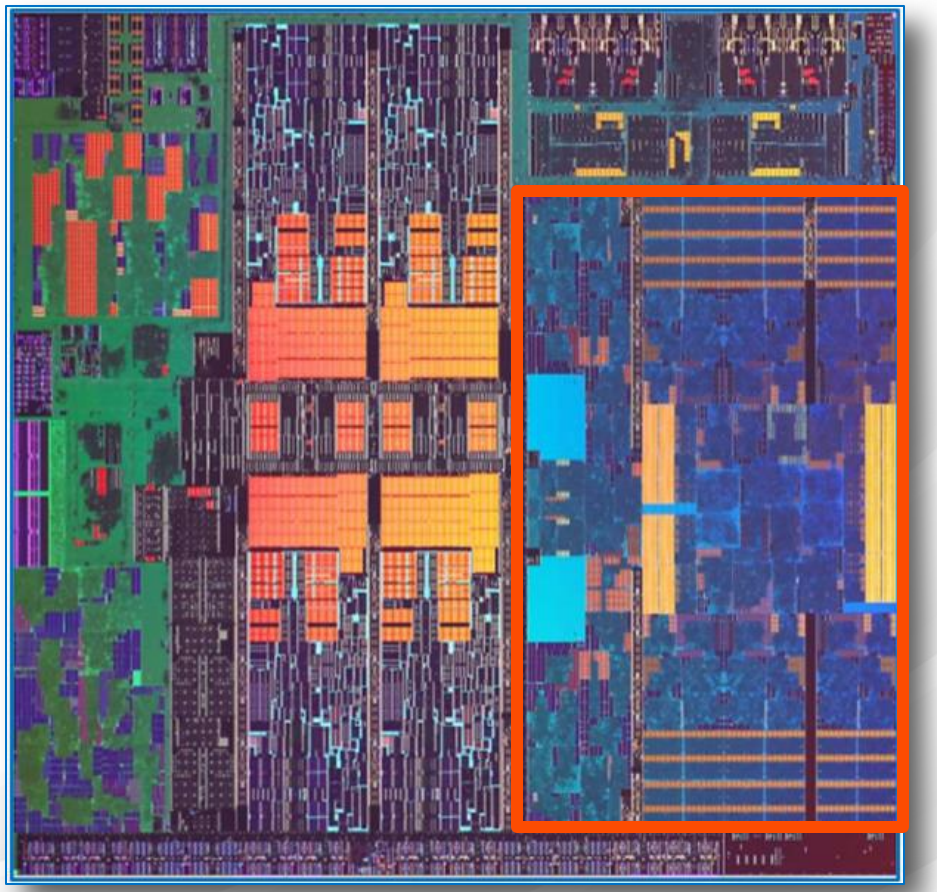
SG1
VISUAL CLOUD FOR GPU STREAMING

Ambitious Goals

~2X 3D/Compute performance

at ~iso-area and ~iso-power

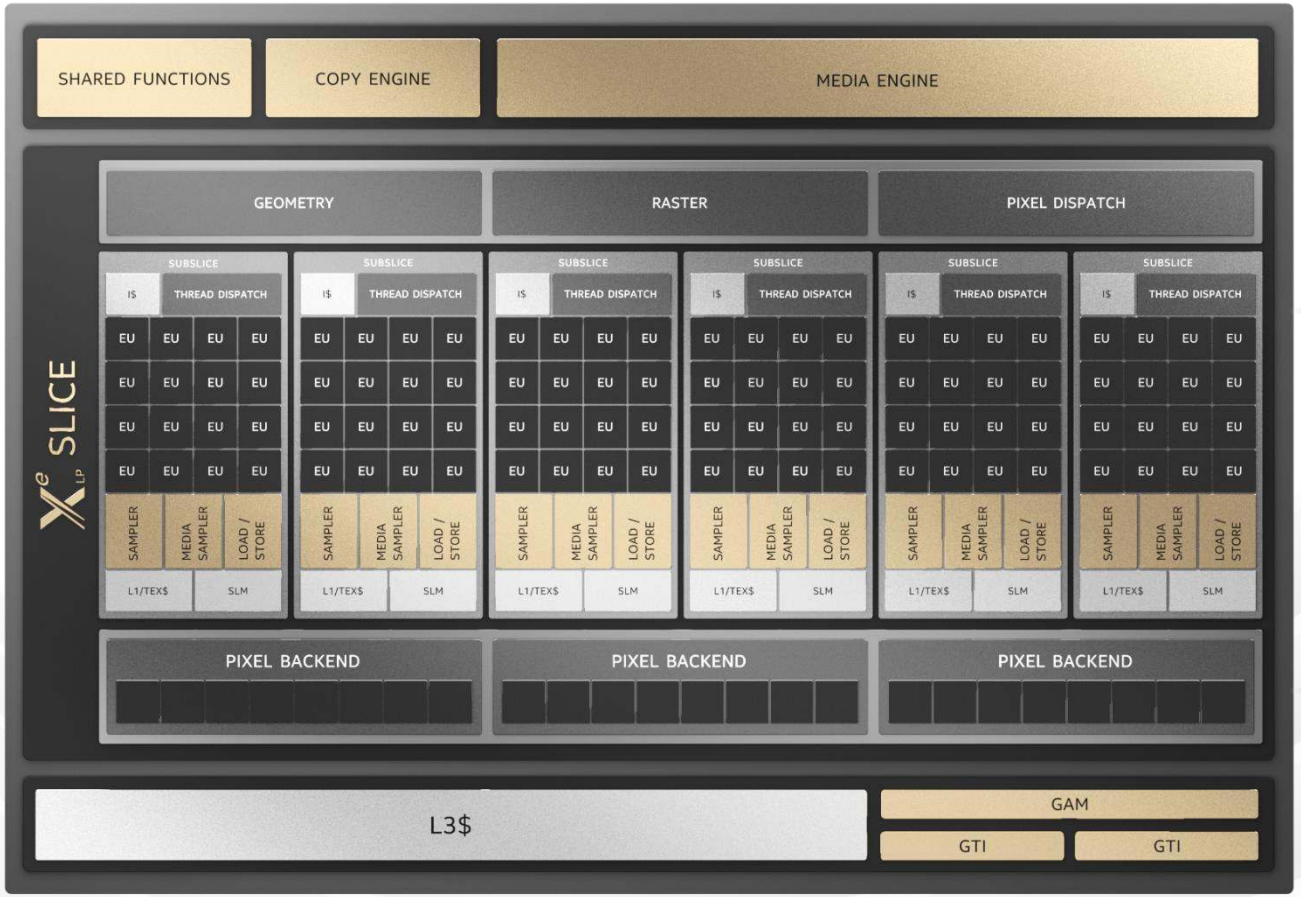
vs. prior generation



Tiger Lake SoC with X^e_{LP} GPU

Xe LP 1.5x Larger Engine

Up to
48 Texels/Clock

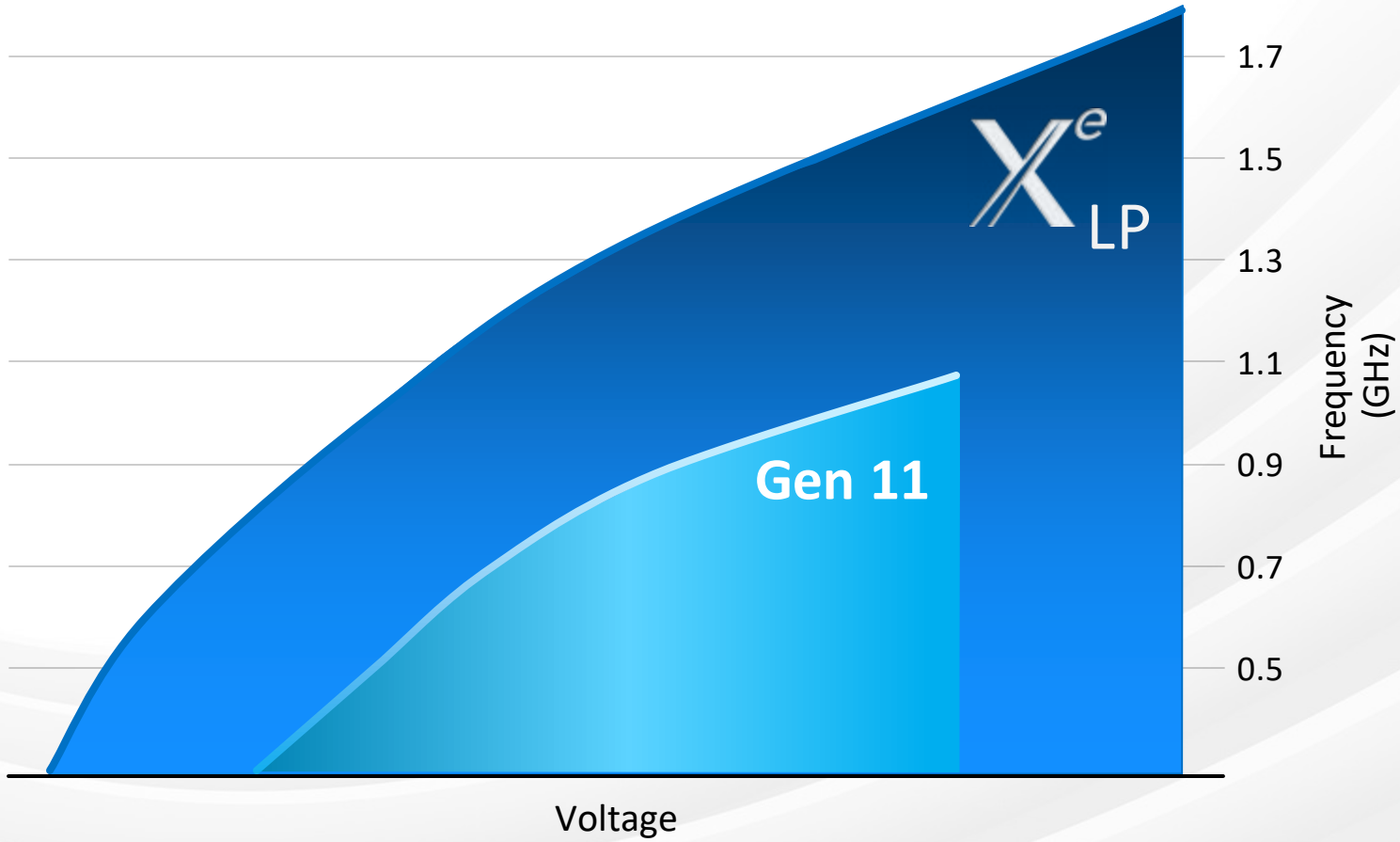


Up to
96 EUs
1536 Flops/Clock

Up to
24 Pixels/Clock

Xe LP Efficiency Improvements

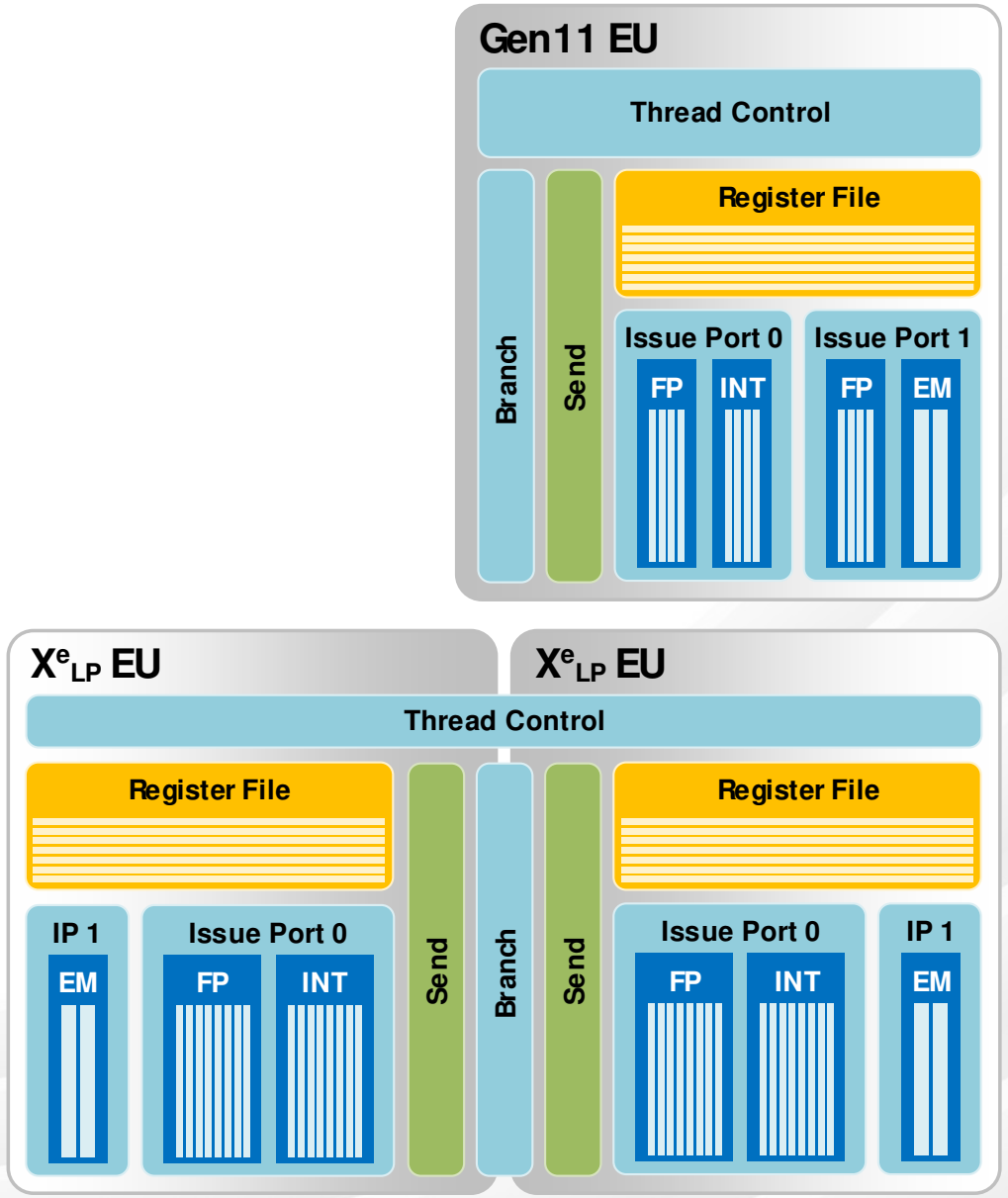
- Frequency uplift at iso voltage
- Greater dynamic range
- Repipelining
- Bottlenecks analysis



Graph for illustrative purposes only

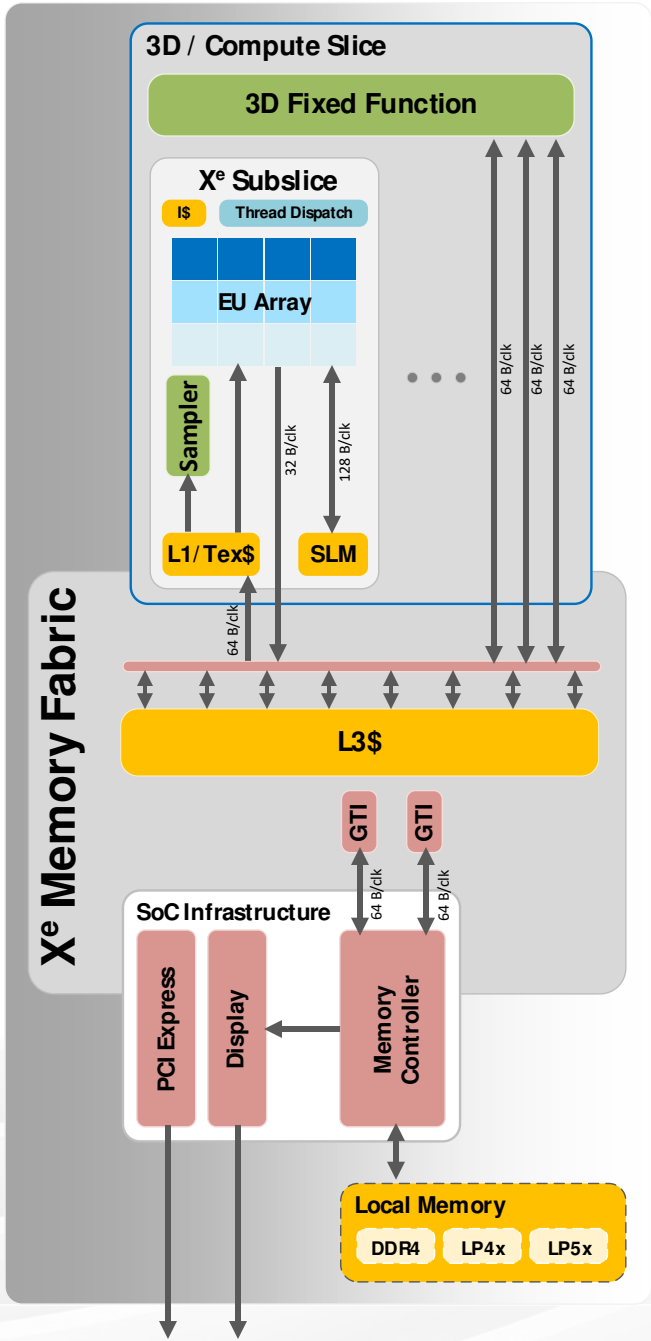
Xe LP Execution Unit

- High-efficiency thread control
  - Software score boarding
  - Pairs of EUs run in lockstep
- 8-wide FP/INT ALU
  - 2x INT16 and INT32 rates
  - Fast INT8 with DP4A
- 2-wide Extended Math ALU



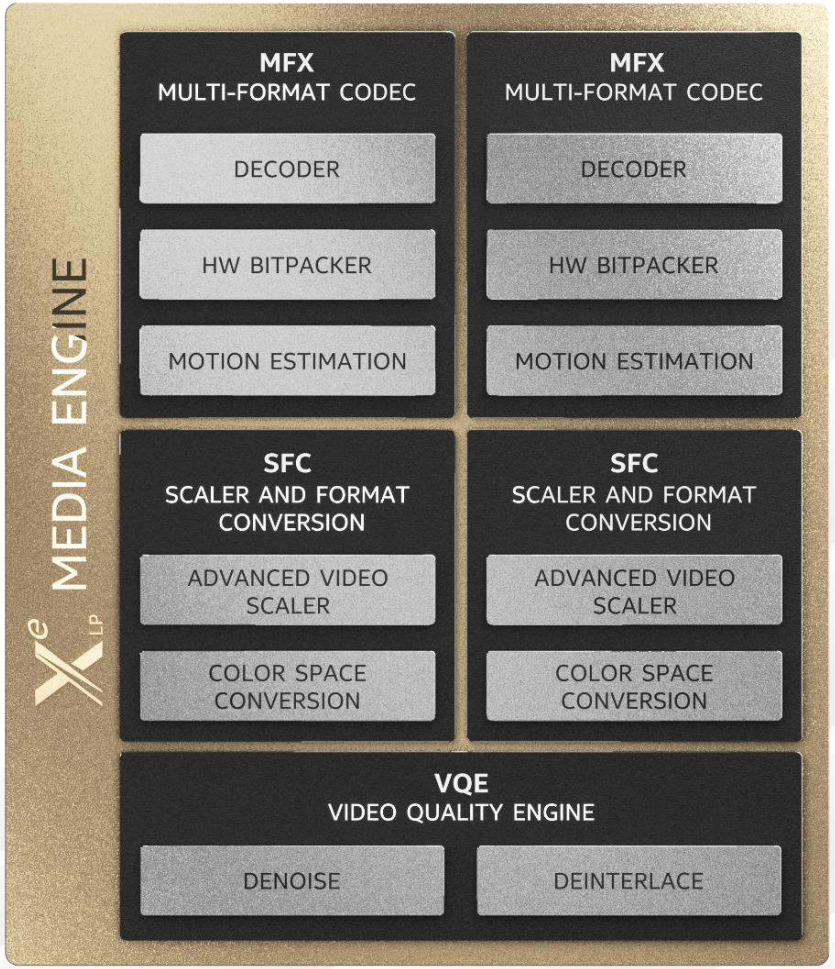
Xe LP Memory System

- New L1 data cache
- Up to 16 MB L3
- 2x GTI bandwidth
- End-to-end compression
- Support for local memory **(optional)**

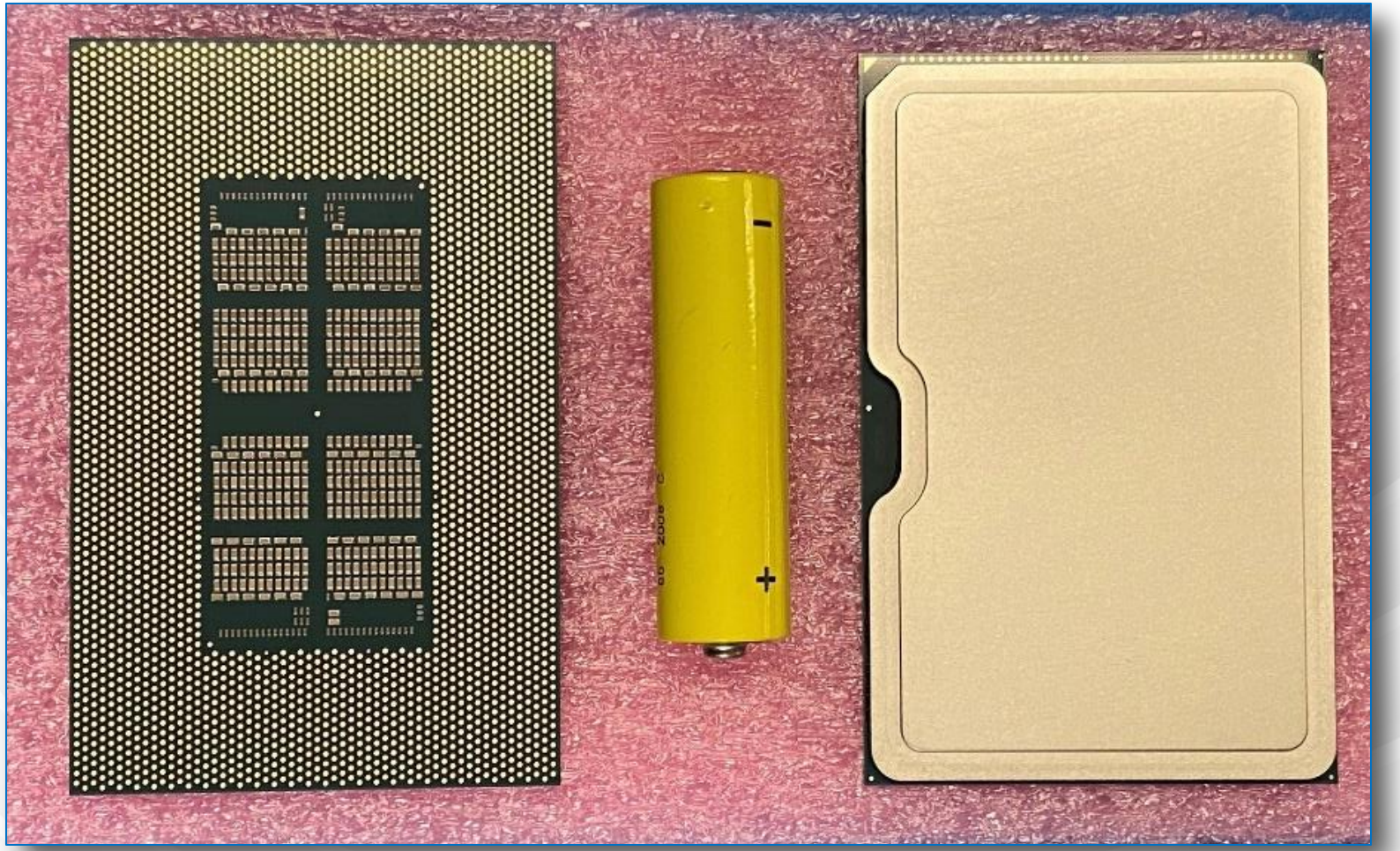


Xe LP Media Engine

- Up to 2x encode/decode throughput
- AV1 decode acceleration
- HEVC screen content coding support
- 4K/8K60 playback
- HDR/Dolby Vision playback
- 12-bit end-to-end video pipeline



Xe HP In the Lab



Xe HP Multi-tile GPU

1-Tile
>10 FP32 TFLOPS

2-Tile
>20 FP32 TFLOPS

4-Tile
>40 FP32 TFLOPS

Building Xe

µArchitecture	Packaging		Process
Xe HPC — PONTE VECCHIO	FOVEROS / CO-EMIB	BASE TILE	Intel 10nm SuperFin
		COMPUTE TILE	Intel Next Gen & External
		RAMBO CACHE TILE	Intel 10nm Enhanced SuperFin
		Xe LINK I/O TILE	External
Xe HP — TBA	EMIB		Intel 10nm Enhanced SuperFin
Xe HPG — TBA	STANDARD		External
Xe LP — SG1, DG1, TIGER LAKE	STANDARD		Intel 10nm SuperFin

Xe Recap

Xe HPC

Highly Configurable as family of microarchitectures

Xe HP

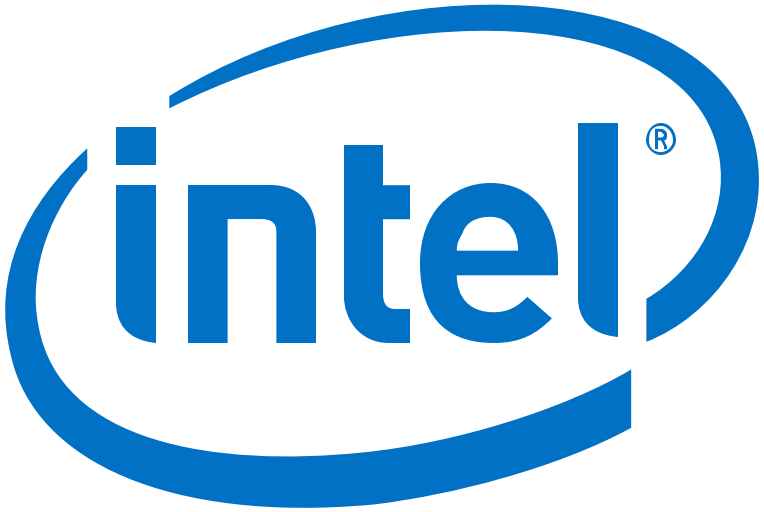
Scalable to 1000s of Execution Units

Xe HPG

New Capabilities across 3D, Compute, Media, Display

Xe LP

Significant Perf/W and Perf/mm2 increases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